Reference text for ACT modulation

Contribution to 802.3dm Task Force

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Contributors

This text proposal was heavily influence by offline discussions with key input from

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Introduction

- There were three modulation schemes proposed in the 802.3dm meeting in Hamburg:

Title	Presenter(s)	Affiliation(s)
Proposed Asymmetrical Modulation	William Lo	Axonne
Asymmetric modulation scheme	Ragnar Jonsson	Marvell
Echo in asymmetric duplex system with spreading	Hossein Sedarat	Ethernovia

- While these were clearly different proposals, they had many things in common, as pointed out in jonsson_3dm_01_10_10_24.pdf
- This presentation describes reference text describing a compromise solution (see jonsson_sedarat_lo_3dm_01_11_11_24_text.pdf)
- The actual text is captured in separate PDF document, based on template from Natalie (see P802d3dm%20draft%20outline%20example%2020241106.pdf)

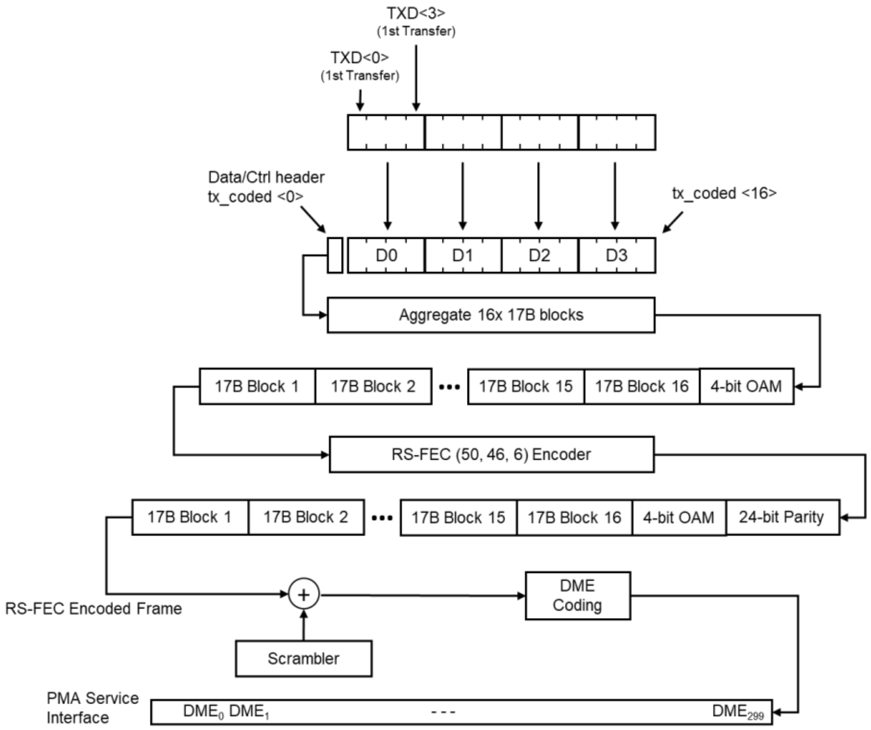
High Level Description

- The proposed ACT modulations support asymmetric data rates with 2.5Gbps, 5Gbps, and 10Gbps in the High Data Rate (HDR) direction and 100Mbps in the Low Data Rate (LDR) direction
- The proposed modulation scheme is based as much as practical on 802.3ch (Clause 149)
- The HDR modulation is the same as defined in 802.3ch (Clause 149)
- The LDR modulation is based on Differential Manchester Encoding
- The intent is to leverage existing 802.3 standards as much as practical

Leverage excising 802.3 standards and eco-system, with only minor addition to 802.3ch

New RS-FEC

- The text proposal includes a new RS(50,46,6) Forward Error Correction (FEC), that is slightly different from what was presented in previous ACT related presentations
- The FEC frame consists of 16 16B/17B blocks, 4 OAM bits, and 24 FEC parity bits
- Each 16B/17B block encodes four 4-bit MII data and control transfers
- This framing has about 17% overhead, resulting in 117.1875Mb/s line rate



Closer Look at RS(50,46,6)

- Latency
  - The RS(50,46,6) FEC will introduce about 2.5-3us latency when FEC decoding is active, which in some applications is higher than desired
  - If the FEC decoding is not active this latency reduces to about 0.4us
- Burst correction
  - The RS(50,46,6) FEC with line rate of 117.1875Mb/s can correct over 50ns error bursts
- Flexibility
  - The text proposal assumes MII with 16B/17B blocks, but the same FEC code could also support XGMII with 64B/65B blocks, if Task Force selects XGMII over MII for low rate
- Complexity
  - The complexity of the FEC decoder is higher than for some of the alternative ACT candidates, but is still a very small portion of the overall PHY complexity

Structure of the Text Document

- The text document is based on a Word document template provided by Natalie, after off-line discussions following invitation on the email reflector (see https://ieee802.org/3/ISAAC/email/msg00284.html)
- Natalie's template document has headers for the various sections needed for the 802.3dm document (see P802d3dm%20draft%20outline%20example%2020241106.pdf)
- The text needs to describe different variants of the PHY link:
  - Three different speeds: 2.5G/100M, 5G/100M, and 10G/100M
  - Two directions: Hight data rate direction (H) and low data rate direction (L)
  - Two cable types: Balanced differential pair (T1) and coaxial cable (V1)
- The text proposed for ACT is highlighted in red in the text proposal document

2xx.1.4 Operation of MULTIG/100MBASE-T1/V1-L/H

- The PCS is described at a high level in Clauses 2xx.1.4.1and 2xx.1.4.2
  - The high data rate direction is based on Clause 149
  - The low data rate direction uses MII, 16/17B block, with RS(50,46,6)
- The PMA is described at a high level in causes 2xx.1.4.3 and 2xx.1.4.4
  - The high data rate direction is based on Clause 149.4
  - The low data rate direction uses 117.1875Mbd
- The Link Sync is described at a high level in causes 2xx.1.6.
  - The link synchronization is only described at a very high level

2xx.1.5 Signaling, -H

MultiG/100M-BASE-T1/V1-H signaling is performed by the PCS generating continuous code-group sequences that the PMA transmits over single balanced pair of conductors (T1) or single coaxial cable (V1). The signaling scheme achieves a number of objectives including:

a) **Forward error correction** (FEC) coded symbol mapping for data.

b) Algorithmic mapping from **TXD<31:0> and TXC<3:0> to PAM4 symbols** in the high speed transmit path.

c) Algorithmic mapping from the received signal on the **MDI port to RXD<31:0> and RXC<3:0>.**

d) **Uncorrelated symbols** in the transmitted symbol stream.

e) **No correlation** between symbol streams traveling both directions.

f) **Block framing** and other control signals.

g) Ability to **signal the status of the local receiver** to the remote PHY to indicate that the local receiver is not operating reliably and requires retraining.

h) Ability to **automatically detect and correct for incorrect polarity in the connection**.

i) Optionally, ability to support refresh, quiet, and alert signaling during LPI operation.

The PHY may operate in three basic modes: the normal data mode, the training mode, or an optional LPI mode.

In high speed direction, the PCS operates according to Clause 149.

2xx.1.6 Signaling, -L

MultiG/100M-BASE-T1/V1-L signaling is performed by the PCS generating continuous code-group sequences that the PMA transmits over single balanced pair of conductors (T1) or single coaxial cable (V1). The signaling scheme achieves a number of objectives including:

a) **Forward error correction** (FEC) coded symbol mapping for data.

b) Algorithmic mapping from **TXD<3:0> and TXC<3:0> to DME** symbols in the high speed transmit path.

c) Algorithmic mapping from the received signal on the **MDI port to RXD<3:0> and RXC<3:0>.**

d) **Uncorrelated symbols** in the transmitted symbol stream.

e) **No correlation** between symbol streams traveling both directions.

f) **Block framing** and other control signals.

g) Ability to **signal the status of the local receiver** to the remote PHY to indicate that the local receiver is not operating reliably and requires retraining.

h) Ability to automatically detect and **correct for incorrect polarity** in the connection.

i) Optionally, ability to support refresh, quiet, and alert signaling during LPI operation.

The PHY may operate in two basic modes: the normal data mode or the training mode.

In low speed direction and normal mode, the PCS generates a continuous stream of DME symbols that are transmitted via the PMA. In training mode, the PCS is directed to generate only TBD_training symbols for transmission by the PMA. (See Figure XXX–32.)

2xx.1.7 Interfaces

All MULTIG/100MBASE-T1/V1-L/H PHY implementations are compatible at the MDI and at the MII/XGMII, if implemented. Implementation of the MII and XGMII is optional. Designers are free to implement circuitry within the PCS and PMA in an application-dependent manner provided that the MDI and MII/XGMII (if the MII/XGMII is implemented) specifications are met. System operation from the perspective of signals at the MDI and management objects are identical whether the MII/XGMII is implemented or not. **The MDI for single balanced pair of conductors (T1) or single coaxial cable (V1) are different**.

2xx.2 MULTIG/100MBASE-T1/V1-H service primitives and interfaces, high speed channel

Service primitives and interfaces the high speed direction are **as described in Clause 149.2.**

2xx.3 MULTIG/100MBASE-T1/V1-L service primitives and interfaces, low speed channel

MultiG/100MBASE-T1/V1-L service interface is as specified in **149.2.2**, with the exceptions given in this subclause:

- MII instead of XGMII
- DME instead of PAM4
- Nominal rate of 117.1875 MHz instead of S x 11250 MHz

2xx.4 Physical Coding Sublayer (PCS) functions, -H

The PCS functions for MultiG/100MBASE-T1/V1-H are as specified for MultiGBASE-T1 PHYs in **149.3**.

2xx.5 Physical Coding Sublayer (PCS) functions, -L

*Similar to **149.3**, except:*

- MII instead of XGMII
- 16B/17B instead of 64B/65B
- RS(50,46,6) instead of RS(360,326,10)
- 4 OAM bits per frame instead of 10
- No interleaving

2xx.6 Physical Medium Attachment (PMA) sublayer, -H

The high speed PMA functions are as specified in **149.4**.

2xx.7 Physical Medium Attachment (PMA) sublayer, -L

*Similar to **149.4**, except:*

- DME instead of PAM4

2xx.8 Physical Medium Dependent (PMD) sublayer, T1

*Similar to **149.5**, except:*

- Also includes PSD for low data rate transmission

2xx.9 Physical Medium Dependent (PMD) sublayer, V1

Still mostly empty, except for

- Transmit PSD for low data rate
- MDI return loss requirements

Summary

- Specific text is proposed for ACT modulation for 802.3dm
- The text is mostly based directly on Clause 149 (802.3ch)
- The text itself is in a separate document, that follows the document structure suggested by Natalie
- This text is based on off-line discussions and is provided to generate further discussion, with the intent of achieving consensus on ACT modulation for 802.3dm
- All comments and suggestions related to this text are greatly appreciated

Comments and Collaborators Wanted

Thank You