Benefits and Tradeoffs of Time Division Duplexing (TDD) over Single-Wire Links

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Outline

- Single-wire link tradeoffs to consider
- Overview of time division duplexing benefits
- Time division duplexing tradeoffs
- Summary

Single-wire links

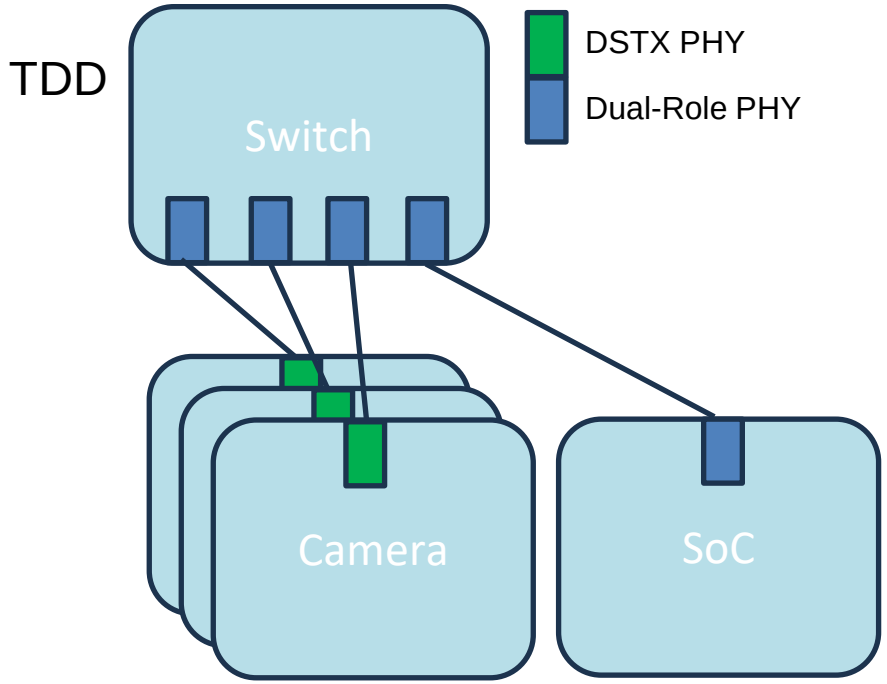
- Single-wire links must operate in a complex environment
- Obvious technical tradeoffs include size, complexity (both direct and indirect), power (direct and indirect), and performance
- Other critical tradeoffs include EMI/EMC, power coupling network, interoperability
- Ease of integration requires careful analysis (SoCs, imagers, and switch/hub)

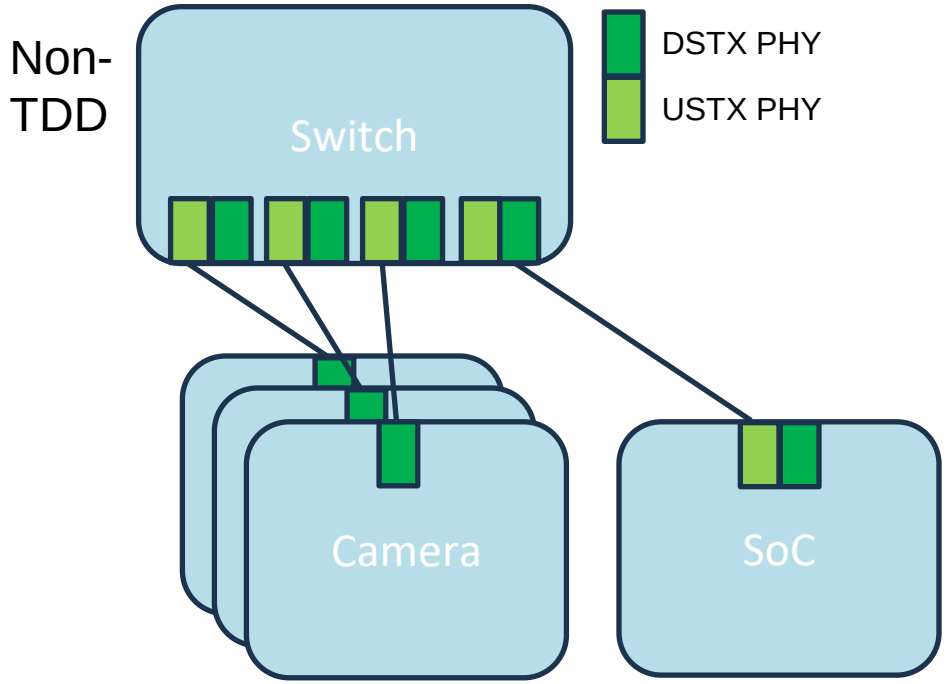
Time Division Duplexing (TDD) Benefits

- **Simplified Design and Lower Complexity:**
  - No simultaneous transmission, No Echo Canceller Required
  - Single Power Coupling Network: TDD uses the same order of magnitude frequency/bandwidth in both directions, allowing the same power coupling network to be used at both ends for all rates.
- **Reduced Power Consumption:**
  - Minimized Transmitted Signal Power: By transmitting one direction at a time, the instantaneous signal power can be minimized.
  - Efficient Use of Bandwidth: TDD can efficiently utilize the available media bandwidth, avoiding additional power to separate frequency bands.
  - Simplified receiver and power coupling also improve camera power efficiency.
  - Peak/instantaneous power is minimized.
- **Enhanced EMI/EMC Performance:**
  - Lower Emissions: TDD avoids simultaneous transmissions, lowering simultaneous emissions.
  - Simplified Analysis and Testing: Single active transmitter at any time simplifies the analysis and testing for compliance, reducing development time and iterations.
- **Interoperability and Integration:**
  - Ease of Integration: TDD's more symmetric design can be efficiently integrated into system-on-chip (SoC) designs, imagers, and switches/hubs. A single SERDES design can perform either upstream or downstream role by changing configuration.
  - Scalability: TDD can be scaled to different data rates and applications without significant changes to the MDI and lower layers.
- **Operational Efficiency:**
  - Single Transmitter and Receiver: The limitation to a single transmitter and receiver active at any time eliminates upstream/downstream signal interactions and improves the reliability of the communication link.
  - Consistent Performance: TDD's use of the same frequency/bandwidth in both directions ensures consistent performance, leading to more predictable and reliable operation.

Integration Considerations

- **Lowest peak power for imager/camera:**
  - Imager performance can be degraded by hot spots, so peak power is more relevant than average power.
  - Camera PHY peak power for TDD is determined by the maximum of TX_POWER or RX_POWER.
  - Camera PHY peak power for non-TDD is TX_POWER+RX_POWER+ECHO_CANCELLER_POWER
- **Dual-role capability:**
  - The PHYs integrated in an SoC or Switch could need to be used as Downstream TX (DSTX) or Upstream TX (USTX) depending on the system.
  - For TDD PHY starting from a support of 2.5G/5G/10G RX and 2.5G TX, an integrated dual-role-capable PHY means adding 5G/10G TX capability.
  - For non-TDD it needs to be investigated if a similar dual-role PHY port is feasible, or if a dual-role port would require integrating 2 different PHY's (USTX) + (DSTX).
  - A dual-role PHY is not required for a camera/imager, but could be used in TDD case.





Addressing Tradeoffs

- **Guard Periods and Bandwidth Efficiency:**
  - Guard Periods: TDD requires guard periods to switch media direction. This will reduce the overall bandwidth efficiency.
  - Bandwidth Utilization: Gbps/Hz suffers, driving higher baud rates.
  - Resolution: Increase transmission speeds to compensate, but save significant receive power, resulting in lower peak power.

- **Latency:**
  - Timeslot Delay: Arbitrated media access contributes to higher latency.
  - Resolution: Choose appropriate TDD intervals to meet application-specific latency requirements. Less than 15us is achievable.

Addressing Tradeoffs

- **Complexity in Timing and Synchronization:**
  - Precise Timing Requirements: TDD requires precise timing coordination between the transmitter and receiver to ensure that they switch modes in sync. This requires additional mechanisms to maintain synchronization in the presence of variable delays or jitter.
  - Synchronization Overhead: Maintaining synchronization can introduce additional overhead, both in terms of processing and potential need for synchronization signals, which can slightly reduce the effective data throughput.
  - Resolution: Leverage existing solutions from ASA. PTB mechanism has been demonstrated to achieve fast time alignment with low overhead.
- **Interference and EMI/EMC Considerations:**
  - Transient Emissions: Without appropriate techniques, the transitions between transmission and reception modes can generate transient emissions.
  - Resolution: Leverage extensively studied and tested solutions from ASA. Measurements have demonstrated meeting these limits is achievable with TDD, appropriate scrambling, resynchronization header dithering, etc.

Summary

- **Compelling Advantages:**
  - Simplified design, lower complexity, and reduced peak power consumption.
  - Enhanced EMI/EMC performance and interoperability.
  - Able to overcome hurdles to integration and dual-role capability.
- **Manageable Tradeoffs:**
  - Challenges can be resolved with appropriate protocol design choices and available solutions as demonstrated by usage in ASA, and that can be leveraged to reduce the risk and timeline for 802.3dm.

- **TDD provides a robust and efficient solution for single-wire point-to-point links that can meet 802.3dm requirements.**
- **TDD PHY can be efficiently integrated in imagers, switches, and SoCs.**

Thank You