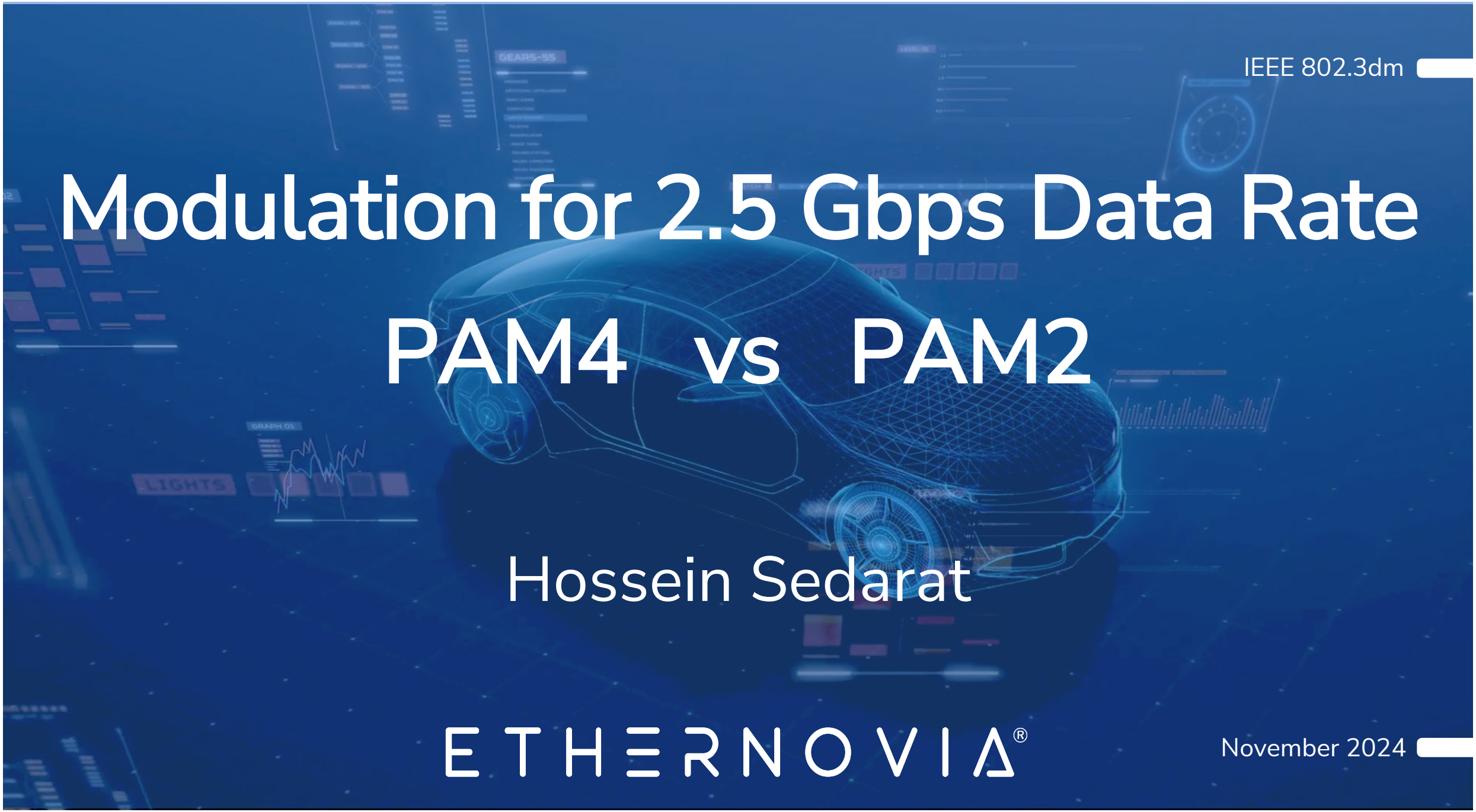
IEEE 802.3dm
Modulation for 2.5 Gbps Data Rate
PAM4 vs PAM2
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ETHERNOVIA®
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# Motivation

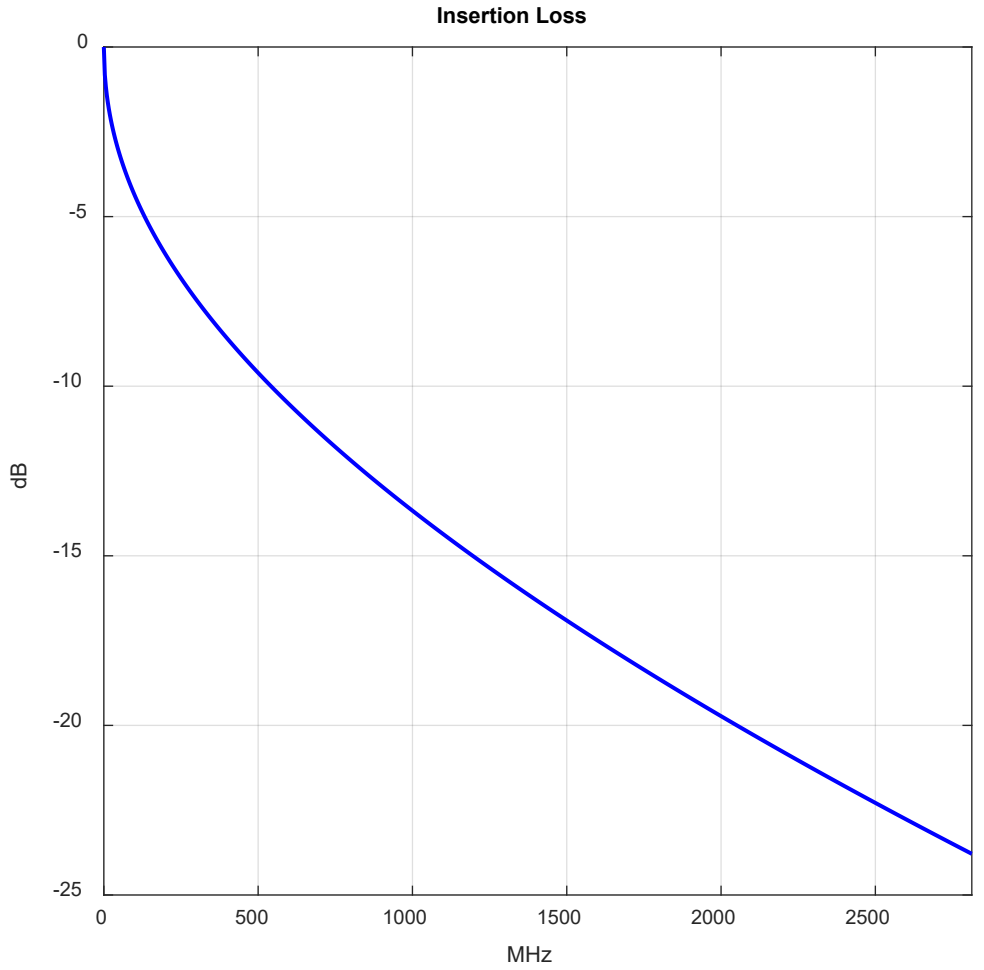
- Using IEEE 802.3ch specifications for downstream direction of 802.3dm offers great benefits:
  - Already ratified through rigorous IEEE adoption process
  - Proven technology with proven interoperability and customer traction
  - Much faster adoption path for 802.3dm
- 802.3ch calls for PAM4 modulation for 2.5 Gbps data rate
- There have been some suggestions that PAM2 may be a better option in 2.5 Gbps mode of 802.3dm
- A comparison of PAM2 and PAM4 is needed

# Outline

- SNR analysis for PAM2 and PAM4
- Complexity comparison
- An overview of EMI
- Conclusions

# Insertion Loss

- At this point, there is no consensus for the limit of insertion loss
- The current proposals seem to suggest a loss of ~24 dB around 2.8 GHz
- This presentation considers a scaled version of 802.3ch limit that meets loss of 24 dB at 2.8 GHz



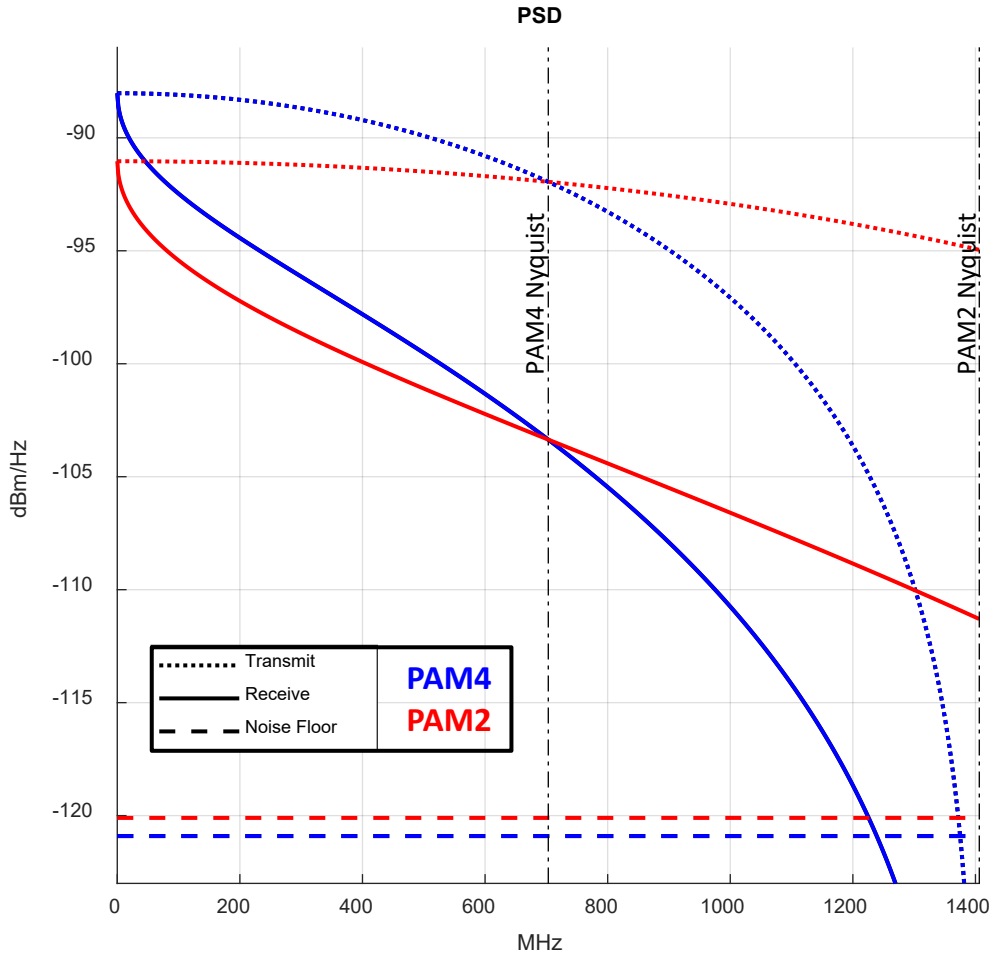
# Target SNR

- BER = $10^{-12}$
- FEC dedicated to non-Gaussian noise sources
- Noise margin = 0 dB

➔ SNR at decision point:
  - PAM2 = 17 dB
  - PAM4 = 24 dB

# Noise Budget

| Salz SNR analysis | | |
|---|---|---|
| **Modulation** | **PAM2** | **PAM4** |
| Symbol Rate (GHz) | 5.625/2 | 5.625/4 |
| Slicer SNR (dB) | 17.0 | 24.0 |
| Tx Power (dBm) | 0.0 | 0.0 |
| Rx Power (dBm) | **-8.9** | **-6.9** |
| Noise Floor (dBm/Hz) | **-120.1** | **-120.9** |
| Input SNR (dB) | **19.7** | **25.6** |



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# PHY Power and Complexity

PHY complexity and power consumption is a complex function of many factors, heavily dependent on architecture, design and implementation techniques

Rough, high-level and general trends:

- Symbol rate: complexity and power grow at least linearly for both analog (sampling rate) and digital (clock frequency) blocks
- Noise budget and dynamic range:
  - Analog: every additional 6 dB of dynamic range results in at least twice the complexity and power consumption
  - Digital: power and complexity grows linearly with dynamic range. 6 dB increase in dynamic range translates to less than 20% more complexity

# Power and Complexity: PAM2 vs PAM4

- Symbol rate: PAM4 = 0.5 * PAM2
  - ➔ power and complexity: PAM4 = 0.5*PAM2
- Noise budget: PAM4 < PAM2 + 6 dB
  - ➔ power and complexity: PAM4 < 2*PAM2

➔ Overall power and complexity: <u>PAM4 < PAM2</u>

# Narrowband Interferers

- The stringent EM immunity requirement demands a robust receiver with adaptive filtering of narrowband interferers
- The legacy analog receivers based on CTLE are suitable only for traditional SERDES applications with no tough immunity requirements
- PAM4 advantages:
  - Receiver needs only half the bandwidth and not exposed to interferers at high frequencies
  - Easier to create high quality notch filters to block narrowband interferers, particularly at lower frequencies
  - Received signal from link-partner is stronger resulting in higher signal-to-interferer ratio and requiring lower relative expansion of headroom

# Summary

- A comparison of two different modulations for 2.5Gbps PHY is presented
- PAM4 receiver is less complex and less power hungry
- A robust automotive receiver requires adaptive notching of narrowband interferers, favoring DSP-based solutions
- PAM4 modulation offers benefits in accommodating and blocking EM interferers

# Conclusion

- For downstream modulation in 2.5G date rate, there is no compelling reason not to use PAM4 as specified by 802.3ch

- Using the IEEE 802.3ch specification in all data rates of 802.3dm in downstream direction offers
  - A high-quality specifications that is approved through rigorous IEEE adoption process
  - A proven technology with proven interoperability and robust customer traction
  - Much faster adoption path for 802.3dm


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