GMSLE Baseline Proposal for IEEE 802.3dm

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802.3dm Task Force Ad Hoc
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Contributors and Supporters

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Outline

- Motivation
- FDD SerDes Baseline
  - Encoding Detail
  - GMSLE vs GMSL3/2
- RL/IL
- Power Spectral Density
  - Downstream PSD
  - Upstream PSD
- Relative Complexity Analysis
- Conclusion

Motivation

- The 802.3dm Task Force is going down two parallel paths, ACT and TDD, with little consensus or convergence
- GMSL3/2 is the Automotive SerDes leader with a proven track record in the field, and has demonstrated EMC and reliability with > 1.1 billion GMSL3/2 links shipped
- Contribute GMSLE (GMSL-Ethernet) proposal to build consensus
- Leverage GMSL while incorporating some of the excellent work done in this Task Force
- Looking for contributors and to build consensus
- This contribution to the .dm Task Force is separate from OpenGMSL
  - If adopted, an implementer does not have to endorse, license, or build an OpenGMSL product

GMSLE FDD SerDes Baseline

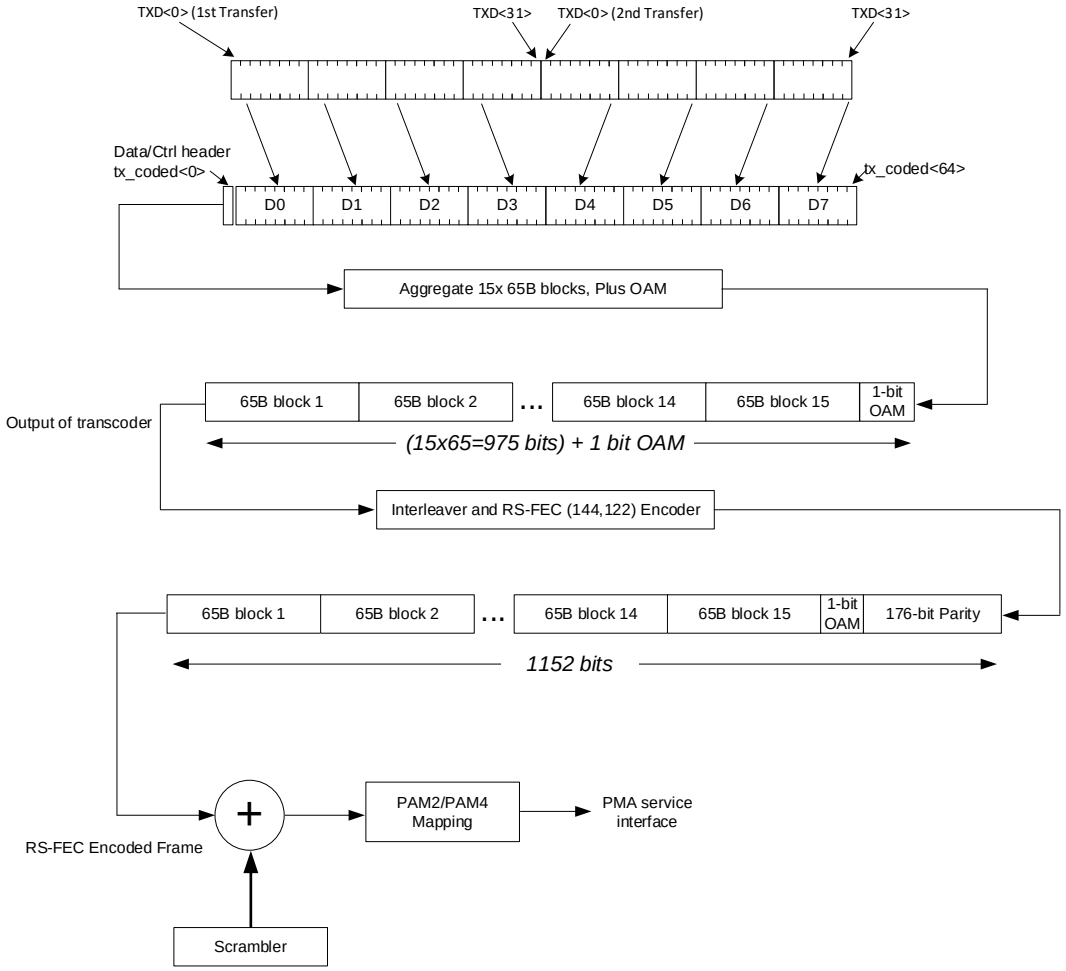
Ethernet MAC Interface	XGMII
Line Coding	64B/65B encoding (see detail, next slide)
Duplexing	FDD with Echo Subtraction/Partial Echo Cancellation
Link Rates and Modulation	Forward Link: 2.5Gbps NRZ, 5Gbps NRZ, 5Gbps PAM4 (option) ,10Gbps PAM4 Reverse Link: 100Mbps
Scrambler	Downstream: $1+x^{13}+x^{33}$ Upstream: $1+x^{20}+x^{33}$

PHY Transmit Parameters

	Rate	Mod	Encoding	FEC RS(n,k)	Baud Rate	TX Power	Burst Noise Protection
Downstream high-speed link rate:	2.5Gbps 5Gbps 5Gbps 10Gbps	**NRZ** **NRZ** **PAM4** **PAM4**	15x65b+1 bit OAM 2x(15x65b+1b OAM) 2x(15x65b+1b OAM) 4x(15x65b+1b OAM)	RS(144,122) L=1 m=8 RS(144,122) L=2 m=8 RS(144,122) L=2 m=8 RS(144,122) L=4 m=8	2.5Gbps: 3GBaud 5Gbps: 6GBaud 5Gbps: 3GBaud 10Gbps: 6GBaud	-4dBm -4dBm -2dBm -2dBm	88 PAM-2 symbols, 29.3ns 176 PAM-2 symbols, 29.3ns 88 PAM-4 symbols, 29.3ns 176 PAM-4 symbols, 29.3ns
Upstream low-speed link rate:	100Mbps	**DME**	3x65b+13bit OAM	RS(30,26) L=1 m=8	100Mbps: 250MHz	-8dBm	16 DME Symbols, 64ns

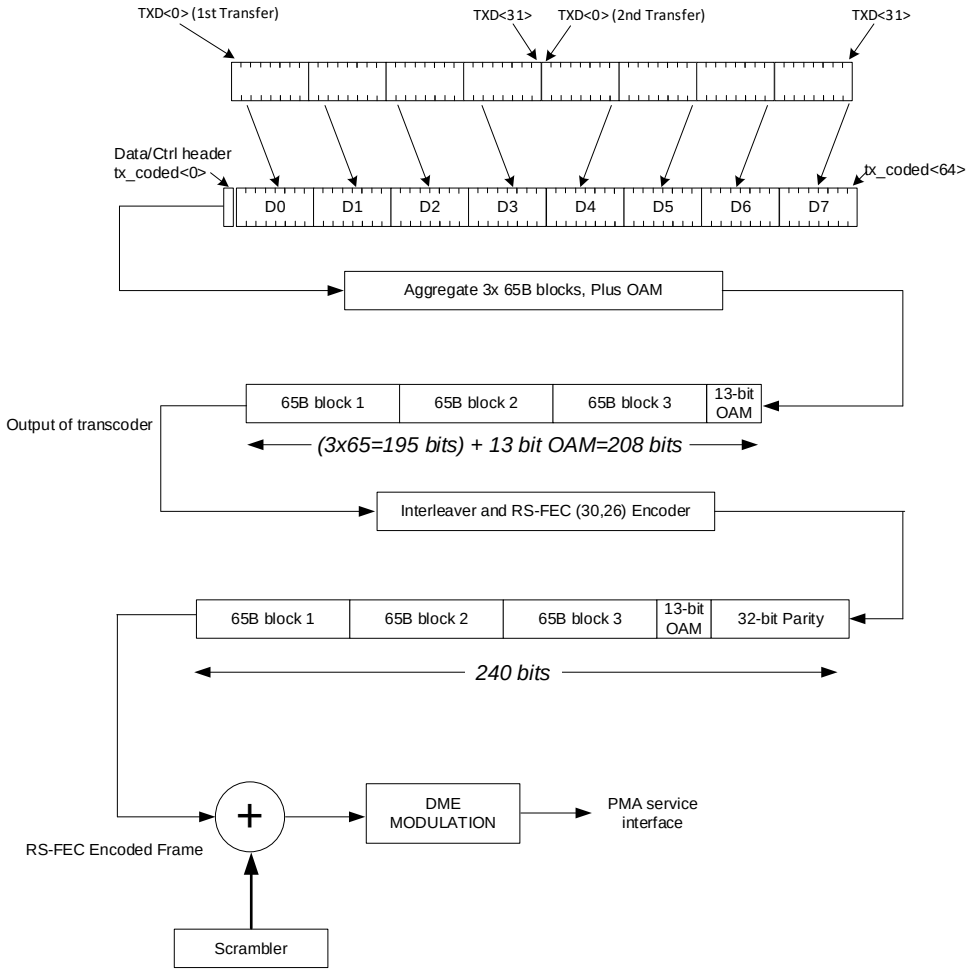
Low complexity POC	Yes, single inductor
XTAL-less Camera PHY?	Yes, supported

Encoding Detail



Downstream High-speed Link

Note: Figure shown for L=1



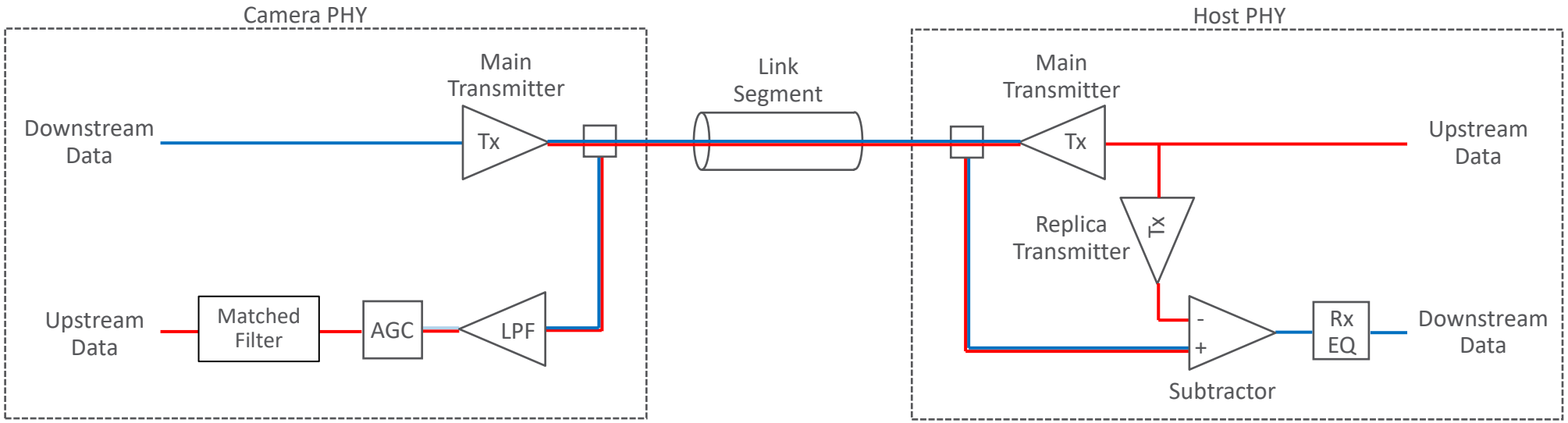
Upstream Low-speed Link

GMSLE Architecture vs GMSL3/2

	GMSLE	GMSL3/2	Notes
Media Interfaces	XGMII	CSI-2	
Line Coding	64B65B	9b10b	9b10b has higher overhead but provides shorter run lengths and DC balance
Transmit Scramblers	Downstream: $1+x^{13}+x^{33}$ Upstream: $1+x^{20}+x^{33}$	Downstream: $1+x^{39}+x^{58}$ Upstream: $1+x^{39}+x^{58}$	
Downstream Baud Rates	3GBaud/6Gbaud	3GBaud/6GBaud	Same Baud rate
Upstream/Reverse	250MBaud DME 100Mbps	187.5MBaud NRZ > 100Mbps	½ bit per Baud with DME
Equalization	Analog CTLE/HPF +DFE Digital also possible	Analog CTLE/HPF +DFE	Same AFE & EQ structure
Downstream/Forward FEC	RS(144,122) L=1/2/4 m=8	RS(128,120) m=8	GMSL3/2 has CRC+ARQ on control channel for FuSa. Ethernet does not have ARQ – need longer FEC length for Ethernet
Upstream/Reverse FEC	RS(30,26) m=8	none	
Sideband channels	Low-rate OAM	I2C, SPI, GPIO, etc.	GMSL3/2 has low latency sideband channels

Duplexing Architecture

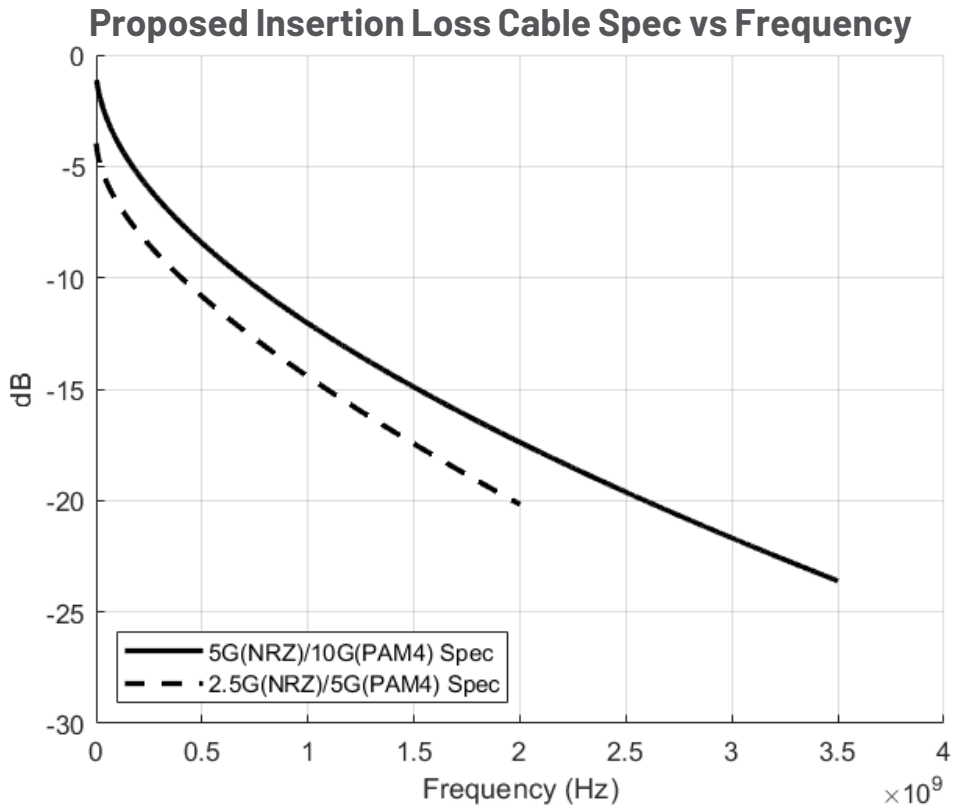
Possible GMSLE Duplexing Implementation



- Echo subtraction is a robust and low-complexity method for duplexing high data rate downstream data and low data rate upstream data on a link segment.
- At the Host PHY, analog hybrid is sufficient – no digital or analog delay line EC is required
- At the Camera PHY
  - Echo subtraction is not required
  - Equalization is not required, a matched filter is sufficient

Proposed Insertion Loss Cable Specification

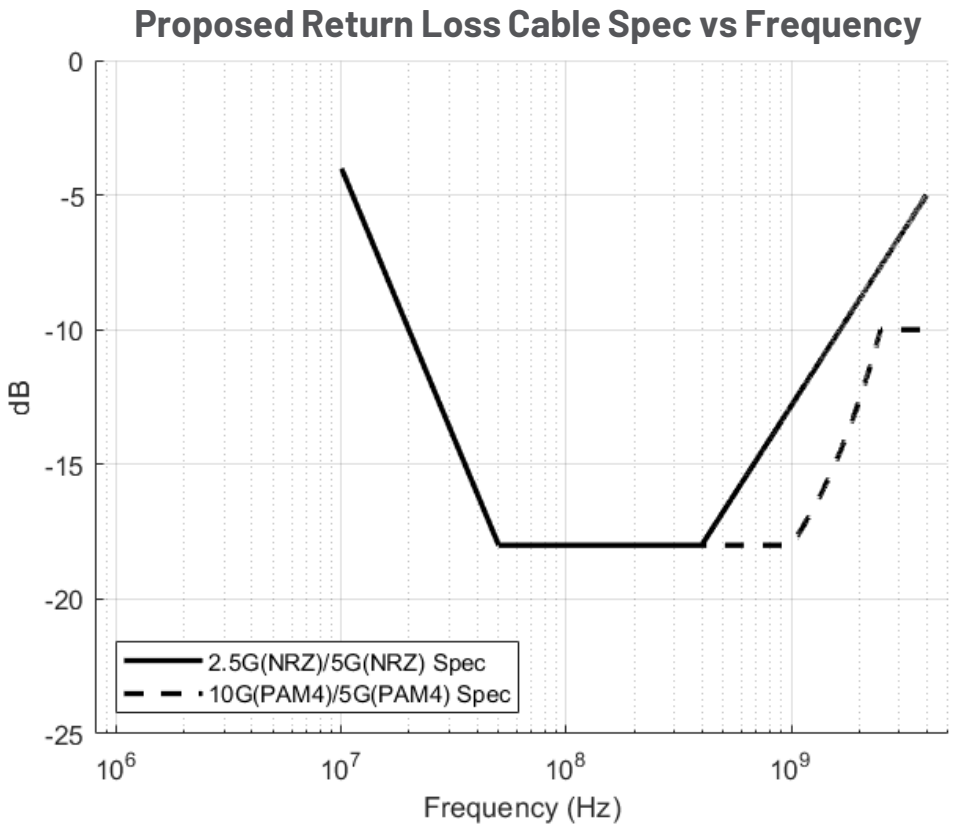
- 15m of coaxial link segment, with up to 4 inline connectors supported
- Propose to adopt Zerna's coax channel insertion loss limit contribution from January interim for 5G(NRZ) and 10G(PAM4) rates [1]
- Add new insertion loss limit for 2.5G(NRZ) & 5G(PAM-4) ending at 2GHz for low cost applications
  - Lower Baud Rate allows more insertion loss for 3MP&5MP cameras while still allowing analog receiver



$$IL_{5G(NRZ)/10G(PAM4)}(f[MHz]) = -\left(0.3 + 0.345\sqrt{f} + 0.000825 * f + \frac{0.48}{\sqrt{f}}\right) \quad for\ 2MHz - 3.5GHz \quad [1]$$

$$IL_{2.5G(NRZ)/5G(PAM4)}(f[MHz]) = -\left(3.7 + 0.27\sqrt{f} + 0.0022 * f\right) \quad for\ 2MHz - 2GHz$$

Proposed Return Loss MDI Specification

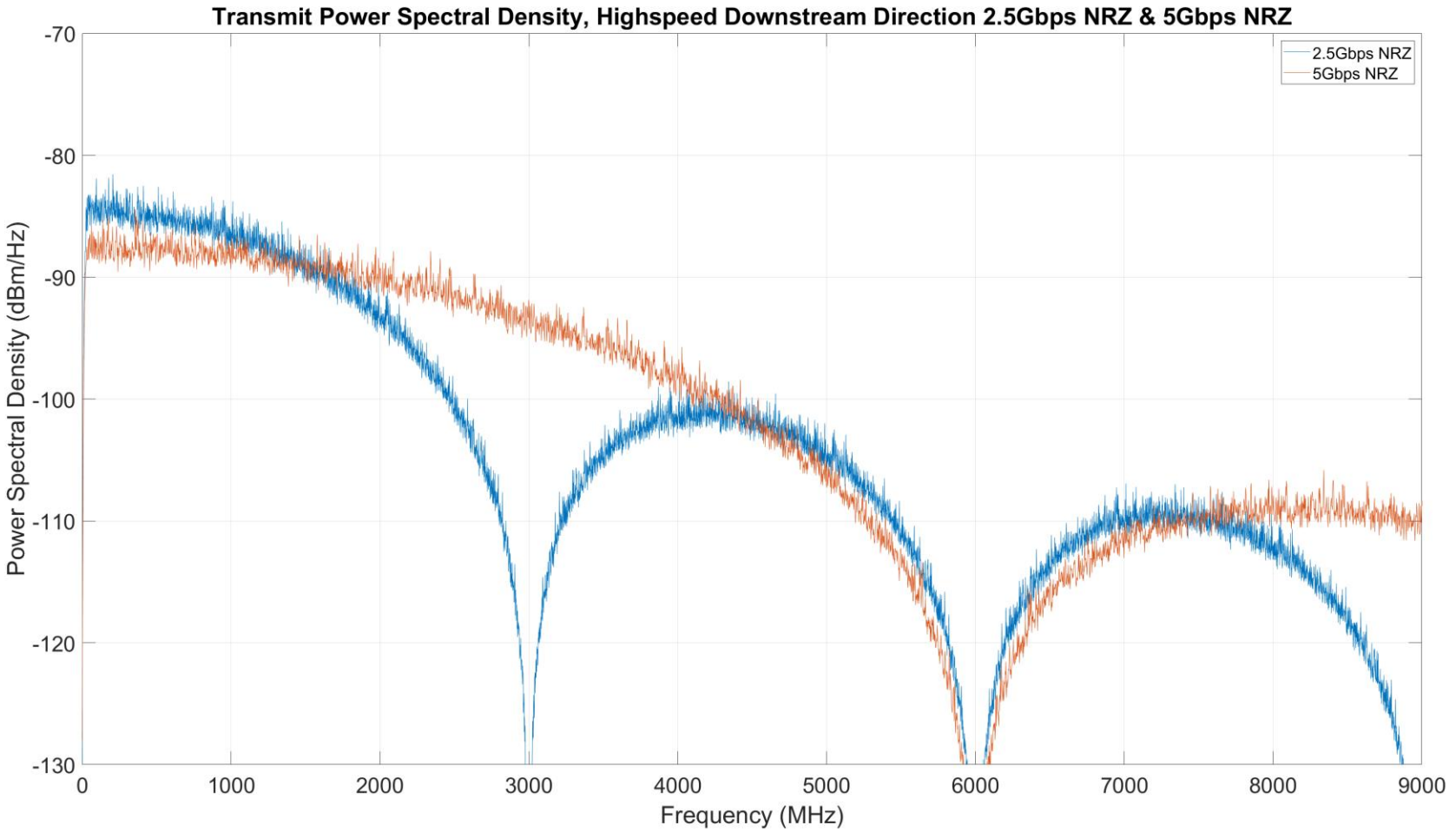


- Use adopted MDI Return Loss Limit for 2.5G(NRZ) and 5G(NRZ) rates, from 10MHz – 4GHz [3]
- Propose extend return loss limit for 5G(PAM4) &10G(PAM4) above 400MHz

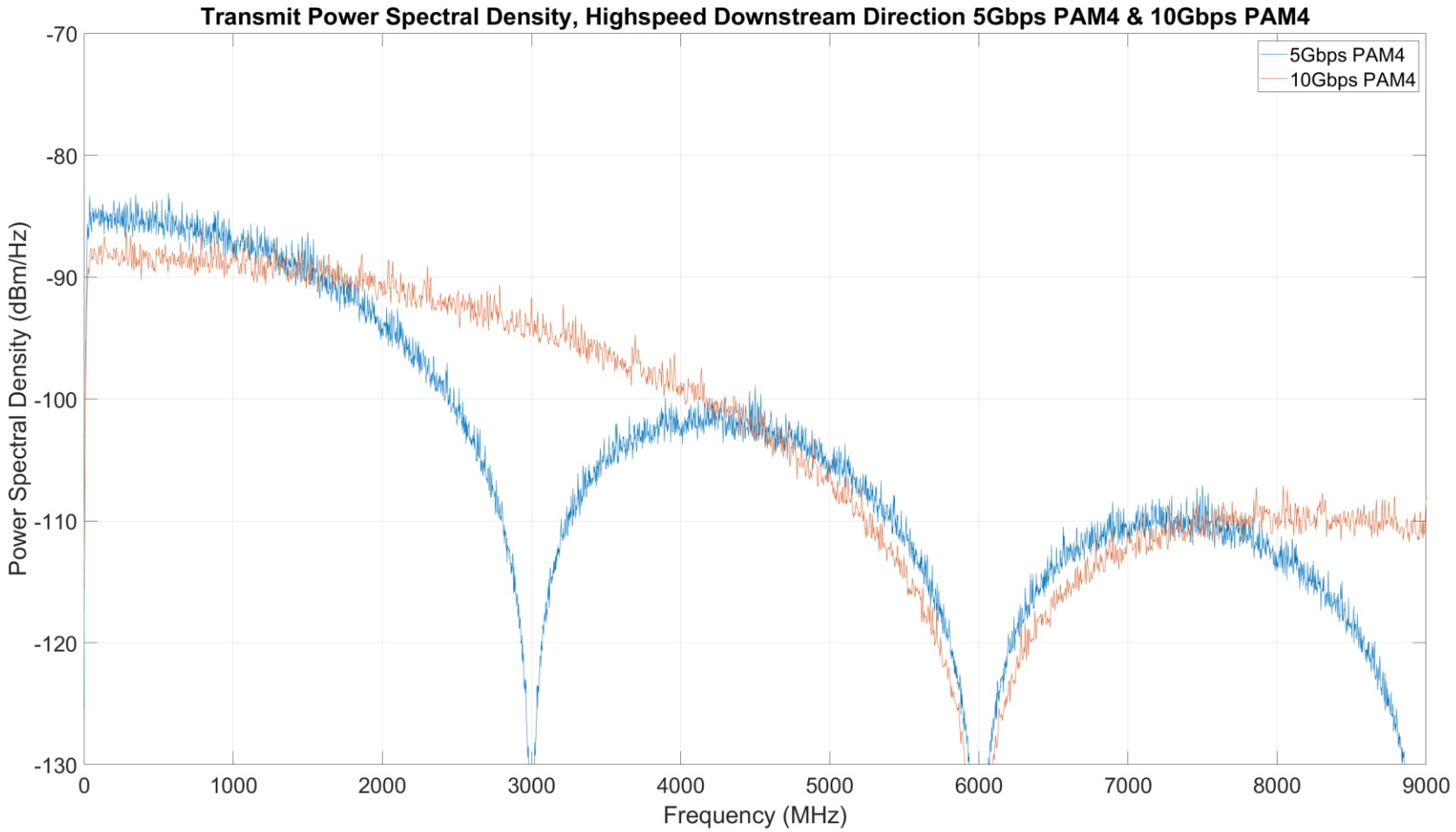
$$RL_{2.5G(NRZ)/5G(NRZ)}(f[MHz]) = \begin{cases} -(18 + 20log_{10}\left(\frac{f}{50}\right) & for\ 10MHz - 50MHz \\ -18 & for\ 50MHz - 400MHz \\ -\left(18\ - 13log_{10}\left(\frac{f}{400}\right)\right) & for\ 400MHz - 4000MHz \end{cases}$$

$$RL_{10G(PAM4)/5G(PAM4)}(f[MHz]) = \begin{cases} -(18 + 20log_{10}\left(\frac{f}{50}\right) & for\ 10MHz - 50MHz \\ -18 & for\ 50MHz - 1000MHz \\ -(23.33 + 0.0053 * f) & for\ 1000MHz - 2500MHz \\ -10 & for\ 2500MHz\ - 4000MHz \end{cases}$$

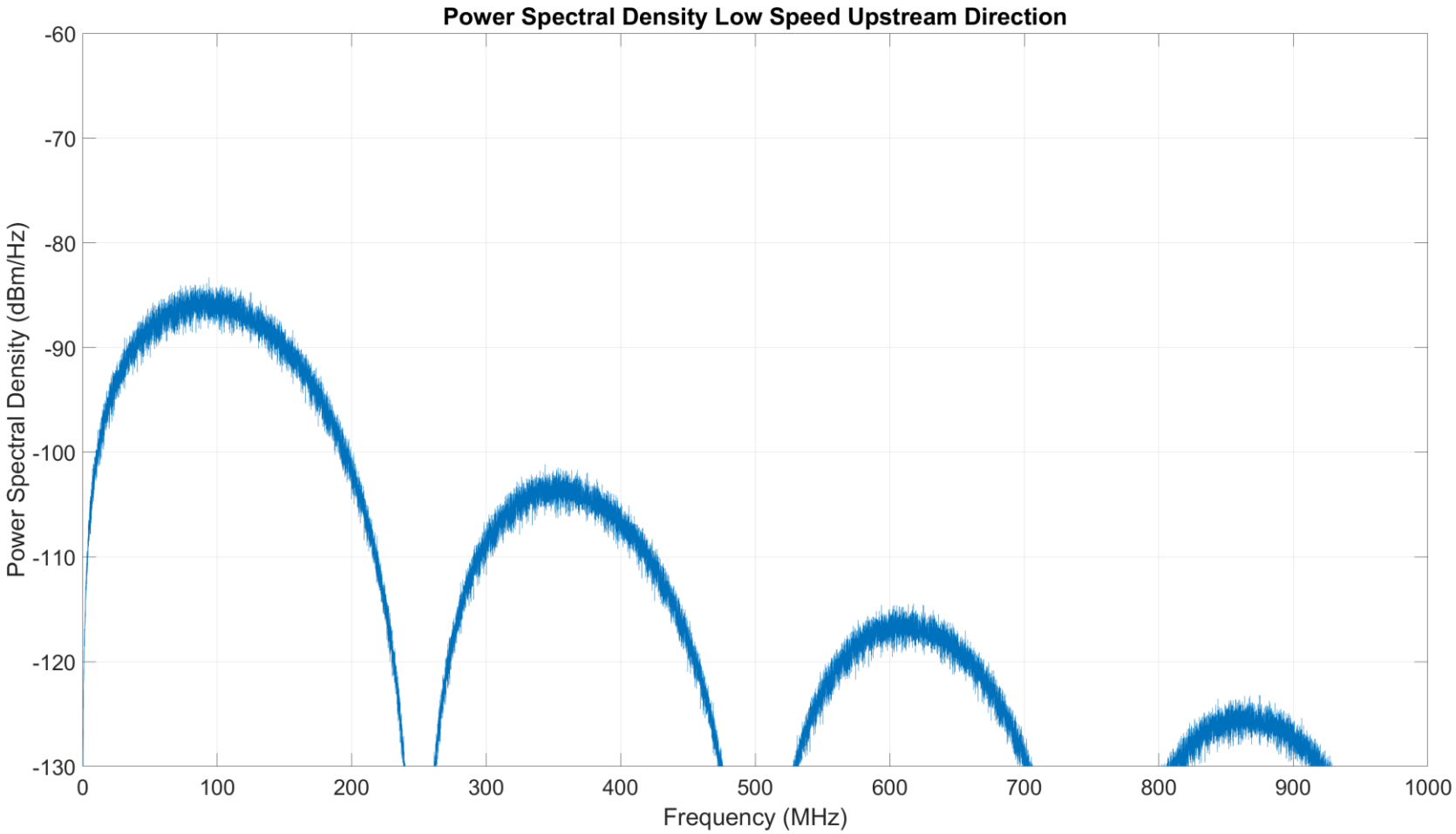
Transmit PSD High Speed Downstream NRZ



Transmit PSD High Speed Downstream PAM-4



Transmit PSD Upstream



Relative Complexity Analysis, Camera PHY

	GMSLE	ACT	TDD
Camera Downstream highspeed TX Complexity	**Least complex** **Lower PAPR** ▪ **2.5Gbps NRZ, 5Gbps NRZ opt.**	Slightly more complex Higher PAPR ▪ PAM4 @ 2.5 & 5Gbps	More complex ▪ TDD
Camera Upstream lowspeed RX Complexity	**Much Less Complex** ▪ **Analog Matched Filter** ▪ **No EQ Required**	**Much Less Complex** ▪ **Analog Matched Filter** ▪ **No EQ Required**	More complex ▪ TDD ▪ Equalization
Camera Power Consumption	**Lowest**	**Lowest**	Highest, Higher Peak Power ▪ TDD ▪ Equalization
Camera LS RX FEC	n=30,k=26, m=8, t=2	n=50, k=46, m=6, t=2	n=130, k=122, m=8, t=4
Camera LS RX FEC decoder area complexity^	1.0x 1 symbol/clock impl @125MHz	**0.71x** 1 syml/clk @117.1875 MHz	**2.66x** Much more complex
Upstream burst protection	**64ns**	51.2ns less than GMSLE	10.6ns much less than GMSLE
Crystal-less Camera Serializer	**Simple** ▪ **Mass production** (GMSL)	Simple	Possible, but more Complex
Upstream latency (including FEC)	8µs	Similar to GMSLE (est)	~9.6µs (est., based on [2])
Summary	▪ **Lowest PAPR** ▪ **Lowest Complexity for 3MP 2.5Gbps and 8Mp 5Gbps cameras** ▪ **Highest burst protection**	Slightly higher PAPR Low Complexity	Highest complexity. Raises cost, power for 3MP 2.5Gbps and 8MP 5Gbps cameras. XTAL-less more complex. Lower burst protection margin with > 2x the complexity

^equivalent area of num 2 input NAND gates + 2-port memory in same geometry ^^(floor((n-k)/2)*m)/Baud

Relative Complexity Analysis, HS RX, LS TX PHY

	GMSLE	ACT	TDD
POC	Small, single inductor	Small, single inductor	**Smallest, single inductor**
Downstream HS Receiver Complexity	**Least complex** ▪ More Euclidean dist. @2.5 Gbps & 5Gbps PAM2 mode ▪ Analog or Digital EQ OK	Most complex ▪ Less Euclidean distance @2.5 & 5 Gbps • Long digital FFE + 1-tap MLSE or DFE (or DFFE)	More complex ▪ TDD
Downstream HS FEC	n=144,k=122, m=8, t=11	n=360,k=326, m=10, t=17	n=130,k=122, m=8, t=4
Downstream HS RX FEC Correctable burst length ^^	29.3ns (L=1,2,4)	**60.4ns** (L=1,2,4 in 2.5/5/10Gbps)	10.6ns (L=1,2,4)
Downstream HS RX FEC Decoder Area Complexity^	1.0x	1.6x	0.66x
Downstream Latency (including FEC)	2.5Gbps: 2.75µs 5Gbps: 1.8µs (L=2) 10Gbps: <2µs (L=4)	2.5Gbps: 4.096µs^^^ 5 Gbps: 2.764µs (L=2) 10Gbps: 2.048µs (L=4)	Claimed 1µs from [2]
Downstream Summary	**Lowest complexity** **Analog or digital EQ OK**	Higher complexity Digital ADC and EQ required	High Complexity, TDD Lower burst noise protection
Reliability (DFMEA)	**Proven**	Limited volume	**Not proven**
Units Shipped	Base architecture (GMSL): **> 1.1 Billion links**	Base architecture (ch): 100k (est.)	0

^equivalent 2 input NAND gates area + two port memory area in same geometry. 750MHz clock in all designs
^^^ from 802.3 clause 149 table 149-20

Conclusion

- GMSLE meets Task Force Objectives
- GMSLE operates with IL and RL limits presented
- GMLSE is the lowest complexity at the camera and the host, of all options presented
- GMSLE builds on GMSL's proven reliability, EMC, and volume shipped
- For the Plenary Meeting we will present:
  - Noise and Emissions Considerations for Coaxial Link Segments, POC measurements and recommendations for 802.3dm
  - Simulation Results with Noise for AWGN, CW, Impulse, and POC noise
- Looking for collaborators and building consensus

References

[1] “Cable Channel IL and RL limits“ Zerna, pp 6
802.3dm Cable Channel IL and RL limits

[2] “TDD Baseline Proposal for 802.3dm“ Chini, Tazebay et al pp 10
TDD Baseline Proposal for 802.3dm

[3] “MDI Return Loss Limit” Jonsson, Chini et all pp 2
Proposed text for MDI Return Loss