

# TDD Fact Checks Assertions vs. Reality



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A Leading Provider of Smart, Connected and Secure Embedded Solutions

**Steve Gorshe**  
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# Supporters

- Scott Muma (Microchip)
- Kamal Dalmia (Aviva Links)
- Ramanjit Ahuja (Onsemi)
- Kirsten Matheus (BMW)

# Introduction

- ❑ **Since the beginning of the IEEE P802.3dm project, a number of assertions have been made against the use of an ASA-like TDD solution. This contribution attempts to examine them in view of what has been learned so far.**
- ❑ **The goal of the contribution is to provide a benchmark for understanding and evaluating the actual TDD proposals under consideration in P802.3dm**

# High-Level

- ❑ High-level assertion: P802.3dm needs a new approach because none of the existing solutions, including ASA, have gained industry acceptance for the target application
  - Fact: While this assertion certainly applies to solutions like GMSL that were already available, it is incorrect to apply it to ASA.
  - ASA components from multiple vendors had just become available and are undergoing testing by multiple OEMs in parallel with the launch and work of P802.3dm
  - There has been significant OEM interest in ASA, and I am not aware of any OEM concerns being raised coming from their ASA tests. For example:
    - [https://ieee802.org/3/dm/public/1124/matheus\\_dm\\_01c\\_pros\\_cons\\_13112024.pdf](https://ieee802.org/3/dm/public/1124/matheus_dm_01c_pros_cons_13112024.pdf)
  - It's unreasonable to declare a technology a “failure” due to lack of deployment when it is just emerging.
- ❑ Fact: TDD contributions can be based on real-world results from actual chips and circuits rather than just questionable simulations

# Latency

- ❑ Assertion: A TDD solution cannot satisfy the  $\leq 10\mu\text{s}$  latency functional safety requirement
  - Fact 1: No contributions have demonstrated the actual need for a  $10\mu\text{s}$  limit, and compelling arguments against this limit have been submitted
    - E.g., in the real application, the PHY latency is dwarfed by the image processing latency:  
[https://iee802.org/3/dm/public/0924/Gollob\\_dm\\_03c\\_System\\_View\\_20240918.pdf](https://iee802.org/3/dm/public/0924/Gollob_dm_03c_System_View_20240918.pdf)
  - Fact 2: In response to latency concerns, TDD supporters have submitted ASA-type TDD formats that fully satisfy the  $10\mu\text{s}$  limit. E.g.:
    - [https://iee802.org/3/dm/public/1124/Dalmia\\_Goel\\_3dm\\_01a\\_11112024.pdf](https://iee802.org/3/dm/public/1124/Dalmia_Goel_3dm_01a_11112024.pdf)
    - [https://iee802.org/3/dm/public/1124/Chini\\_3dm\\_01a\\_1124.pdf](https://iee802.org/3/dm/public/1124/Chini_3dm_01a_1124.pdf)
    - [https://iee802.org/3/dm/public/0125/Chini\\_3dm\\_01a\\_0125.pdf](https://iee802.org/3/dm/public/0125/Chini_3dm_01a_0125.pdf)
- Conclusion: Since ACT claimed a similar  $10\mu\text{s}$  latency, there is no tangible difference between ACT and TDD
  - This assertion should be retired

# PoC, including inductors

- ❑ Assertion: TDD will need multiple and larger inductors than ACT
  - Fact: I am aware of multiple actual ASA-ML implementations that perform very well with a single small inductor.
    - In fact, simulations presented in multiple contributions indicated that it would be much more difficult for ACT to use a single small inductor. E.g.:
      - [https://iee802.org/3/dm/public/0924/Chini\\_Tazebay\\_3dm\\_01a\\_0924.pdf](https://iee802.org/3/dm/public/0924/Chini_Tazebay_3dm_01a_0924.pdf)
      - [https://iee802.org/3/dm/public/1124/Kleinwaechter\\_dm\\_PoC\\_inductors\\_Nov24.pdf](https://iee802.org/3/dm/public/1124/Kleinwaechter_dm_PoC_inductors_Nov24.pdf)
      - [https://iee802.org/3/dm/public/1124/Chini\\_3dm\\_01a\\_1124.pdf](https://iee802.org/3/dm/public/1124/Chini_3dm_01a_1124.pdf)
      - [https://iee802.org/3/dm/public/0924/jingcong\\_dm\\_2024Sep\\_v2.pdf](https://iee802.org/3/dm/public/0924/jingcong_dm_2024Sep_v2.pdf)
  - I am not aware of actual working single inductor PoC models of ACT
  - Conclusion: TDD has been demonstrated to work with a single small inductor in actual circuits, and it is incumbent ACT to demonstrate similar real-world capability

# EMC / EMI

## ❑ Assertion: EMI is a drawback for TDD

- Fact: I am aware of existing TDD solutions that demonstrate no EMI problems in actual OEM evaluations, e.g.:
  - [https://iee802.org/3/dm/public/1124/matheus\\_dm\\_01c\\_pros\\_cons\\_13112024.pdf](https://iee802.org/3/dm/public/1124/matheus_dm_01c_pros_cons_13112024.pdf)
- Due to simultaneous US and DS transmission, it appears that ACT is more likely to have EMI issues
  - [https://iee802.org/3/dm/public/1124/muma\\_3dm\\_01\\_2411.pdf](https://iee802.org/3/dm/public/1124/muma_3dm_01_2411.pdf)
- Conclusion: Claims of TDD EMI problems are unsubstantiated, and claims of better performance for ACT have yet to be proven

# Jitter

- ❑ Assertion: TDD solutions will have jitter performance problems
  - Fact: This assertion has yet to be demonstrated
  - Other contributions have questioned whether ACT based on no crystal or echo-canceller at the receiver can satisfy the SoC-side jitter performance
    - [https://iee802.org/3/dm/public/1124/gorshe\\_3dm\\_01a\\_2411.pdf](https://iee802.org/3/dm/public/1124/gorshe_3dm_01a_2411.pdf)
  - Conclusion: Jitter performance for both solutions need further demonstration



# Packet transfer limitations

- ❑ Assertion: The nature of TDD bursts limit the maximum packet size to being the size of the burst
  - Fact: This assertion implies a fundamental misunderstanding of TDM technology.
    - As demonstrated in countless deployed TDM systems, a TDM channel (e.g., the 8-bit OTN TDM tributary slot channels), including with TDD bursts, is simply a channel of a specified bit rate.
  - Conclusion: Assertions of this nature are counter-productive to progress

# Packet transfer limitations (continued)

- ❑ Corollary Assertion: TDD requires a PHY buffer for a full 1500-byte maximum packet size
  - Fact: Since TDD is simply providing a TDM channel, as explained above, there is no reason to buffer entire packets.
  - At some point within the MAC or between the MAC and the media, TDD does require enough buffering (FIFO depth) to accommodate the number of client data bits that arrive during the time period when there is no TDD burst transmission in that direction.
  - Conclusion: Since this is implementation dependent, there has been no consensus regarding if or to what extent this adds complexity

# Need for a crystal on the camera side

- ❑ Assertion: TDD is not able to support crystal-less operation at the camera side
  - The assertion is based on the TDD not having an US received signal during the DS burst transmission
  - Fact: TDD bursts begin on a highly accurate regular time period. The burst period provides the basic PLL sync and would be adequate in itself.
    - The received bit rate during the US burst provides additional rate information.
    - [https://iee802.org/3/dm/public/1124/Dalmia\\_Goel\\_3dm\\_01a\\_11112024.pdf](https://iee802.org/3/dm/public/1124/Dalmia_Goel_3dm_01a_11112024.pdf)
    - [https://iee802.org/3/dm/public/1124/Chini\\_3dm\\_01a\\_1124.pdf](https://iee802.org/3/dm/public/1124/Chini_3dm_01a_1124.pdf)
  - As noted above on the jitter performance slide, ACT performance without a crystal is not clear.
  - Summary and conclusions:
    - There are no concrete technical grounds for this assertion against TDD
    - Both TDD and ACT are relying on simulations to support the feasibility

# Camera-side complexity

- ❑ Assertion #1: It is difficult or impossible to integrate TDD with the imager
  - The basis for this assertion is unclear
    - It assumes a strawman TDD implementation that does not correspond to any actual implementations of which I am aware
  - Fact: The current TDD proposals use the same symbol rate for US and DS, which should make TDD simpler to integrate than ACT with its different symbol rates.
    - [https://iee802.org/3/dm/public/1124/muma\\_3dm\\_01\\_2411.pdf](https://iee802.org/3/dm/public/1124/muma_3dm_01_2411.pdf)
  - Conclusion: This assertion is disproven by actual working implementations

# Camera-side complexity (continued)

- ❑ Assertion #2: The TDD circuit at the camera side would be “200% bigger than ACT”
  - The assertion, made in two contributions, claims that a TDD receiver would need a hybrid circuit and would need multiple parallel digital data paths with the IC
  - Facts:
    - TDD has no inherent need for a hybrid circuit.
      - ACT implementations, however, may need one
    - I am not aware of any of the existing ASA TDD implementations using such a complex parallel data path and have not been able to find anyone considering one.
    - In fact, TDD allows using a simple analog front end and inherently has no need for an echo canceller.
    - While it has been claimed that ACT can use a simple analog receiver with no DSP-based equalizer or echo canceller, this is questionable and remains to be proven
      - Contributed simulation results indicate that this would have potential problems
        - [https://iee802.org/3/dm/public/0125/ahuja\\_8023dm\\_01a\\_011325\\_on\\_upstream\\_receiver\\_design\\_and\\_performance\\_ACT.pdf](https://iee802.org/3/dm/public/0125/ahuja_8023dm_01a_011325_on_upstream_receiver_design_and_performance_ACT.pdf)
  - Summary: This assertion is unfounded.
    - It is based on a theoretical strawman implementation that does not correspond to known actual implementations

# Conclusions

- ❑ **Each of the primary assertions regarding TDD issues has been subsequently disproven**
  - In most cases, this has been demonstrated in actual ASA implementations that are being evaluated by OEMs
  - In other cases, they have been disproven through simulation results
  - In the remaining cases, both TDD and ACT are relying on simulations to claim similar capabilities that will need to be verified
  
- ❑ **To reiterate: TDD performance has been demonstrated in existing implementations from multiple vendors in independent labs.**
  - In contrast, ACT can only rely on simulations for which there is often a lack of consensus regarding the assumptions.

# Thank You