

August 7th, 2024

System level Discussion

Presenter: Max Turner (max.turner@ieee.org)

Project: IEEE P802.3dm - ISAAC

Event: ISAAC Use Case AdHoc Call

Contribution to:  IEEE

IEEE P802.3dm Task Force - ISAAC

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Presentations considered

- https://www.ieee802.org/3/dm/public/0724/matheus_dm_02b_latency_07152024.pdf
- https://www.ieee802.org/3/dm/public/0724/veloso_dm_01_07152024_v2.pdf
- https://www.ieee802.org/3/dm/public/0724/houck_fuller_3dm_01_0724.pdf

From: houck_fuller_3dm_01_0724.pdf

Latency and Initialization Time are Related

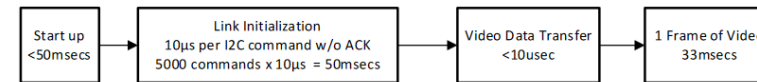
- Initialization is mandated by regulations, and user experience demands better.
 - Meeting government regulations does not meet customer expectations and is consider a “D-” user experience – barely passing system.
 - The NHTSA has established rules regarding rearview camera systems under FMVSS No.111 which focuses on rear visibility
 - The regulations mandate that rearview camera systems must be operational within 2 seconds of the vehicle being placed in reverse
 - Although the standard specifically applies to rearview cameras, it highlights the importance of quick initialization across the various camera systems in vehicles
- Current ADAS sensors can require 1000s to 10000 of initialization commands – Startup time multiplies latency 1000-10000 fold!

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Link Latency Budget Calculation

- Additional latency will accumulate quickly.
- Customers expect 1st frame in <300msecs
 - As more sensors are added customer expects quicker initialization
- Example Total Link Budget Impact




Total Budget to achieve 1st Frame of data = 133.01msecs

Increasing link budget time impacts overall processing cycle timing budget

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https://www.ieee802.org/3/dm/public/0724/houck_fuller_3dm_01_0724.pdf

Contribution to: 

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MT comments on houck_fuller_3dm_01_0724.pdf p. 4/5

- Start-up time should NOT be mixed with Latency or Delay of the data transport
- We should agree on defined terminology in order to prevent misunderstanding:
 - Start up time
 - Image frame transfer latency
 - Ethernet frame latency
 - PHY delay
 - Link delay
 - ...

MT ideas on the use of the “Delay” and “Latency” suffixes

- ‘something’ Delay: “first bit to first bit”
 - Time interval between the (first bit of the) SFD (or any other defined bit) of two packets to pass a certain reference plane
 - Time interval for a certain specified bit within a packet to pass from one reference plane to another reference plane
 - **Does NOT depend on packet length!** i.e. not dominated by line rate
- ‘something’ Latency: “first bit to last bit”
 - Time interval between the (first bit of the) SFD and the (last bit of the) FCS of a certain packet to pass a certain reference plane
 - Time interval between the (first bit of the) SFD of one packet and the (last bit of the) FCS of a response packet to pass a certain reference plane
 - **Depends on packet length!** i.e. dominated by line rate at least for large packets
- More detailed proposal later in the presentation

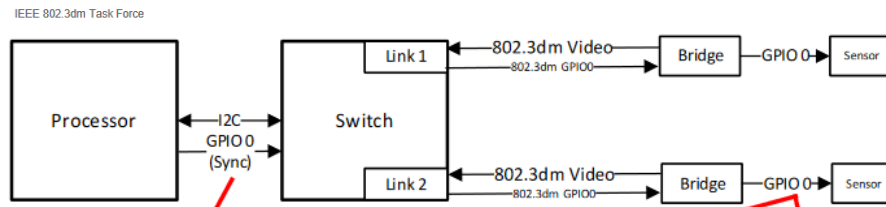
MT questions on: houck_fuller_3dm_01_0724.pdf – p. 6/7

Latency Requirements

- Latency and Jitter are important to avoid long initializations of sensors and frame synchronization with other ADAS sensors
 - There is a 10us hard limit related to functional safety (from switch to camera)
 - This includes a GPIO trigger event or a single I2C command
 - There is a less than 1.0us latency limit from the sensor to switch
 - There is a 1-2us limit on GPIO trigger events from the switch to sensor
 - There is a less than 1.0us latency limit on the video channel from sensor to switch
- Competing SERDES technology can already achieve these latency requirements


MT questions:

- Can we add a reference for each of those requirements on page 6?
- Can we find terms (Bridge, Switch) which are not already overloaded in the 802.1 realm?



page 7

https://www.ieee802.org/3/dm/public/0724/houck_fuller_3dm_01_0724.pdf

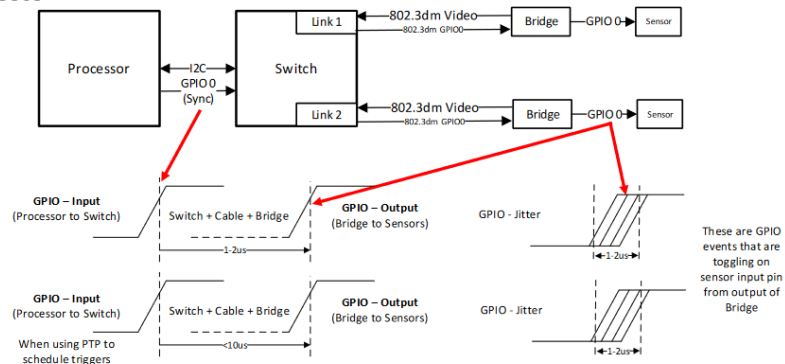
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MT questions on: houck_fuller_3dm_01_0724.pdf – p. 7

Latency and Jitter Application Diagram

- ADAS High Precision applications involving fast moving objects require highly accurate distance and velocity measurements, a trigger latency of $<1-2\mu\text{s}$ is ideal
 - This requires precision synchronization for accurate distance calculations 1 Horizontal Line of accuracy between sensors.
 - PTP can be used to schedule events and provide additional latency on the GPIO trigger if a link can not achieve $<1-2\mu\text{s}$




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MT questions:

- Does this implicitly restrict the topology to a single MDI to MDI link?
- The GPIO-Jitter looks like an application layer problem, not a network problem

https://www.ieee802.org/3/dm/public/0724/houck_fuller_3dm_01_0724.pdf

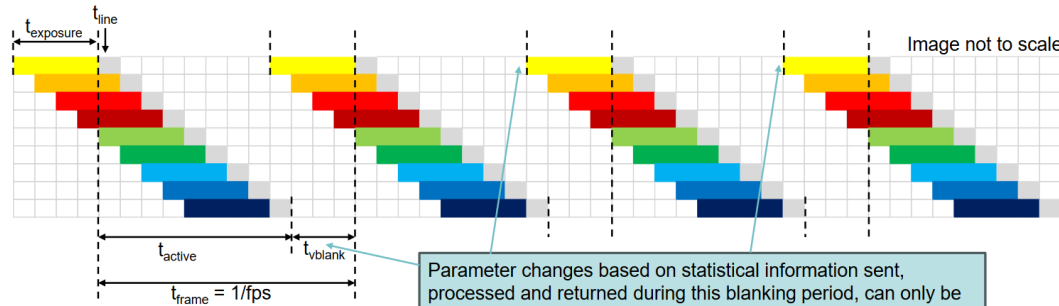
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From: matheus_dm_02b_latency_07152024.pdf

Rolling*) shutter imager timing example

*) Global shutter takes the complete image at once, stores it and then line-wise transfers it. More costly and therefore less common.



Parameter changes based on statistical information sent, processed and returned during this blanking period, can only be applied to the image capture after next. If handling takes longer, the new parameters get applied to yet one image later.

Example:

Frame rate = 30 fps \rightarrow $t_{frame} = 33.3$ ms

Active image = 29 ms (design decision $< t_{frame}$) means $(33.3-29)/29 = \sim 15\%$ blanking overhead

$t_{line} = t_{active} / \# \text{ active lines (imager capability)} = 29 \text{ ms} / 2160 = 13.4 \text{ } \mu\text{s} \ll \text{any other time in the system}$

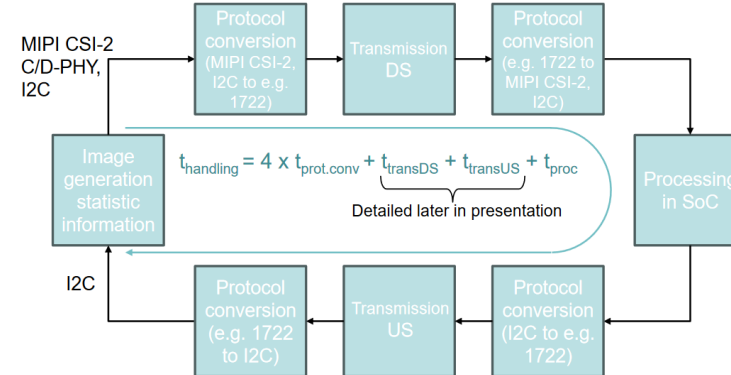
$t_{exposure} = \text{variable (but } < t_{frame} \text{)! } 10 \text{ ms is a typical upper value for 8Mpx}$

$t_{vblank} = 33.3 \text{ ms} - 29 \text{ ms} = 4.33 \text{ ms} > t_{handling1}, t_{handling2} < 37.66 \text{ ms} = 4.33 \text{ ms} + 33.3 \text{ ms}$

\rightarrow Ethernet latencies of 10us in the DS and of 100us in the US are sufficiently small for $t_{handling}$.

Camera application latencies

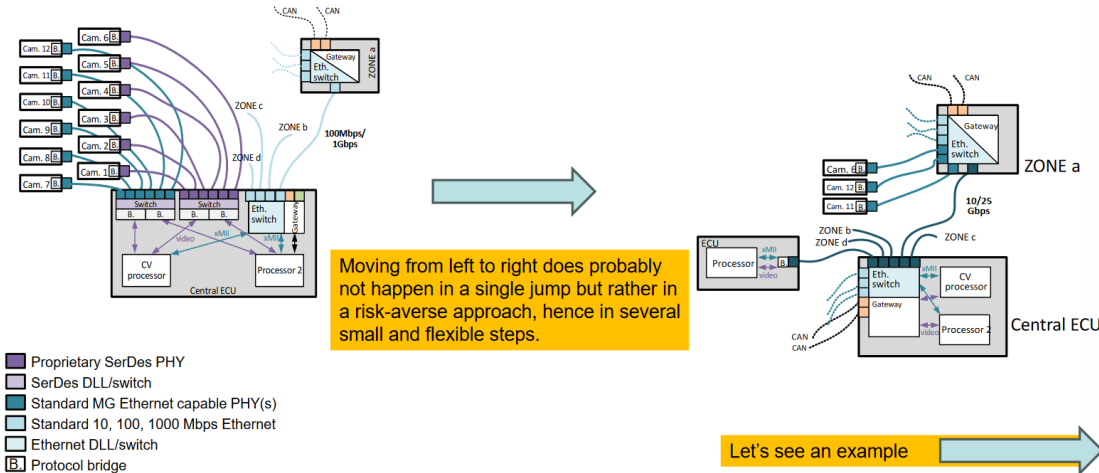
Automotive camera communication typically distinguishes between uni-directional video data and bi-directional control data communication. US latencies are relevant for control data only.



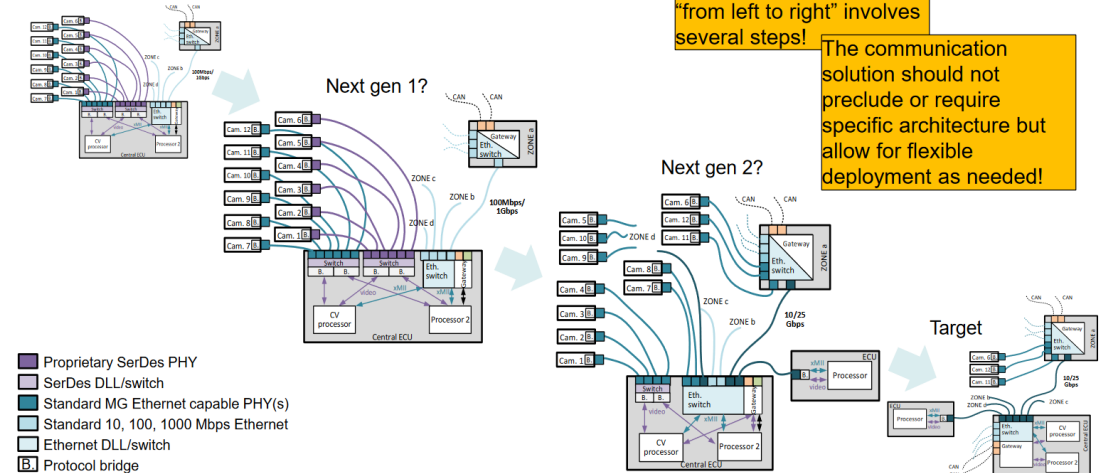
https://www.ieee802.org/3/dm/public/0724/matheus_dm_02b_latency_07152024.pdf

From: veloso_dm_01_07152024_v2.pdf

Introduction: Customer paradox (1)



Introduction: Customer paradox (2)



MT suggested conclusions

- The dot3dm project should NOT:
 - Assume the camera to be directly (MDI to MDI) connected to the receiver/controller
 - Assume the camera to be either global or rolling shutter
 - Make assumptions about processing and forwarding times which are out of the TGs control; e.g. bridges, SOCs, ISPs, other network links
- The dot3dm project should:
 - Assume the camera to be connected to a bridged 802 network
 - Design a generic Ethernet (802.3 MAC and 802.1) compatible PHY for packet transport
 - Optimize the PHY timing behaviour to what is economically and technically feasible



Latency vs. Delay

An attempt to introduce more consistent wording

Denoting Interfaces

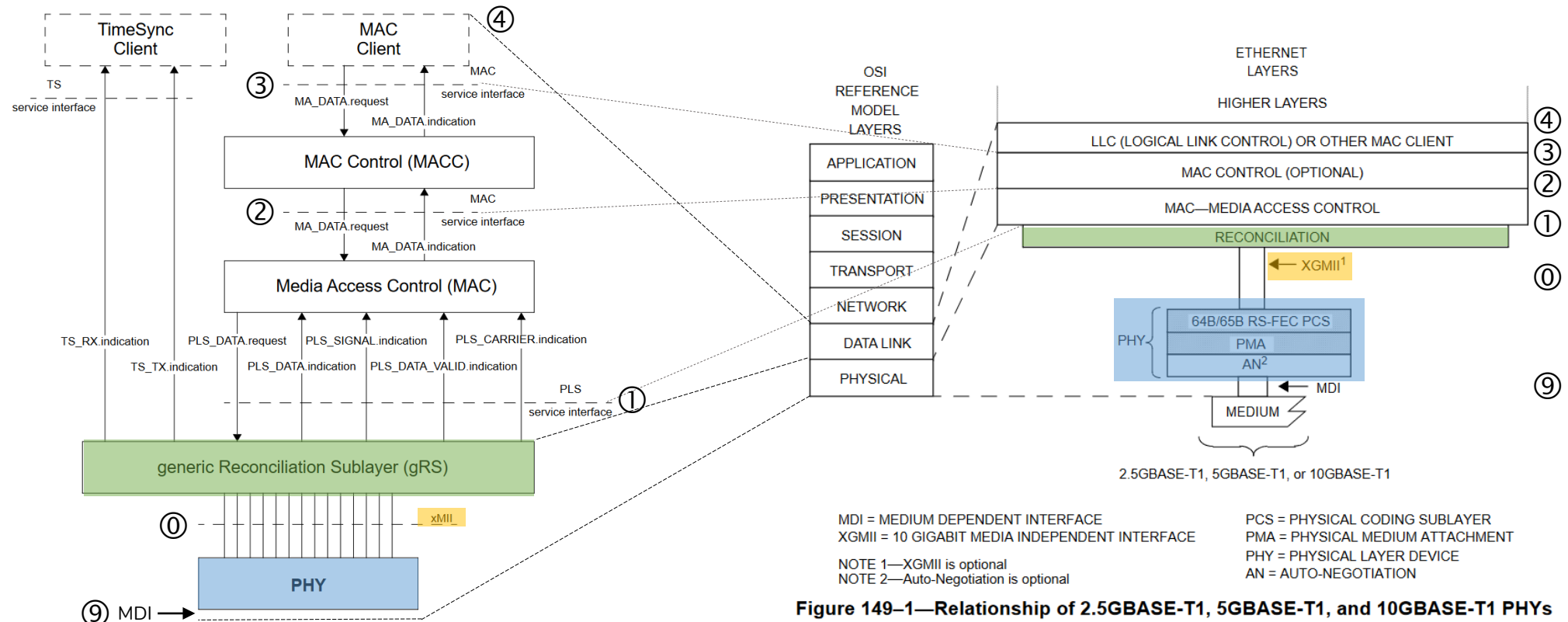


Figure 90–1—Relationship of the TimeSync Client, TSSI and gRS sublayer relative to MAC and MAC Client and associated interfaces

Figure 149–1—Relationship of 2.5GBASE-T1, 5GBASE-T1, and 10GBASE-T1 PHYs to the ISO/IEC OSI reference model and the IEEE 802.3 Ethernet Model

Timestamp Point and Reference Plane

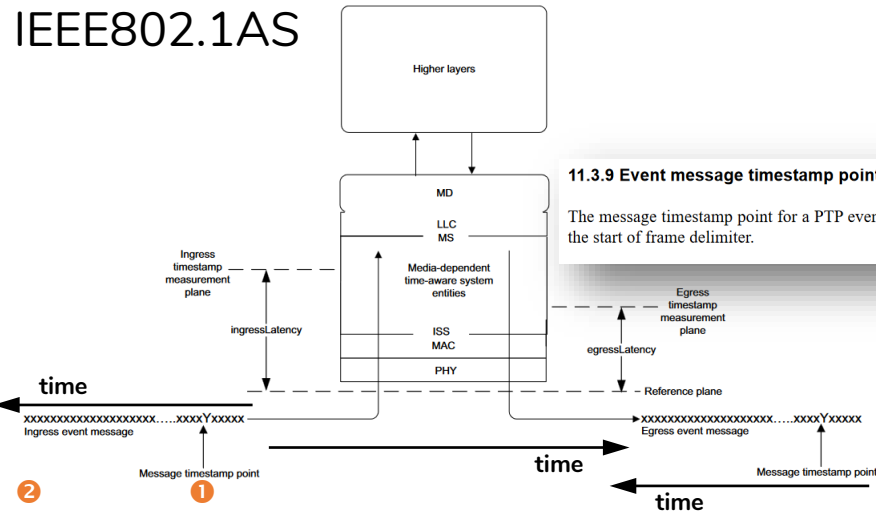


Figure 8-2—Definition of message timestamp point, reference plane, timestamp measurement plane, and latency constants

IEEE802.3

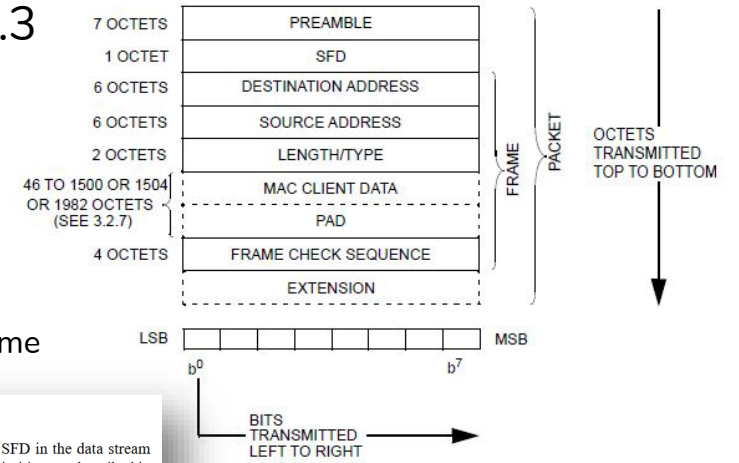
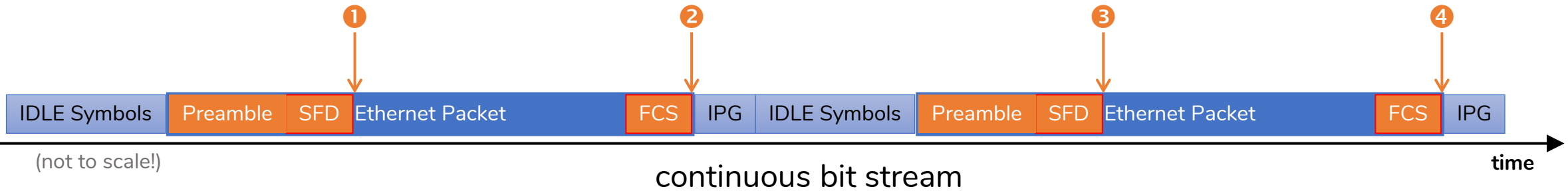


Figure 3-1—Packet format

IEEE802.3: 90. Ethernet support for time synchronization protocols

90.4.3.2.2 Condition for generation

This primitive is generated by the gRS sublayer in response to detection of a valid SFD in the data stream received across the xMII receive signals. Specific conditions for generation of this primitive are described in 90.5.2.



gRS – MII – PHY

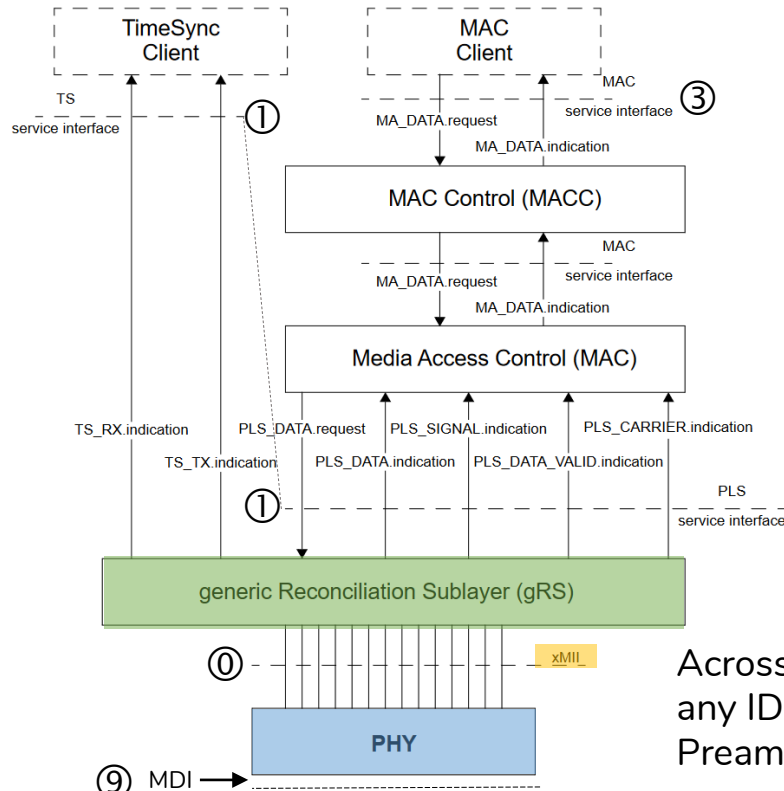
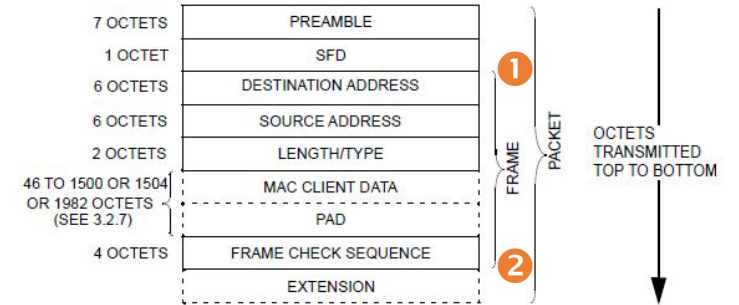
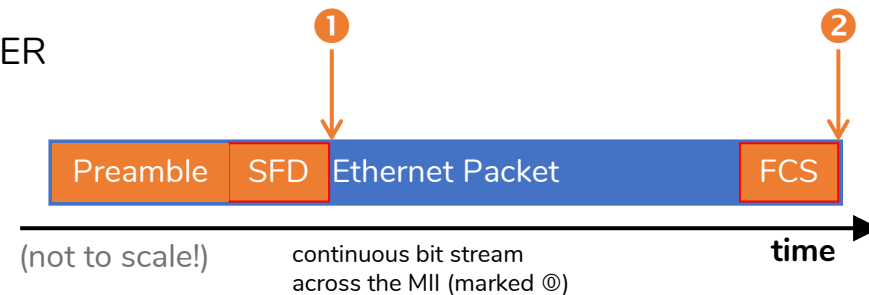


Figure 90-1—Relationship of the TimeSync Client, TSSI and gRS sublayer relative to MAC and MAC Client and associated interfaces

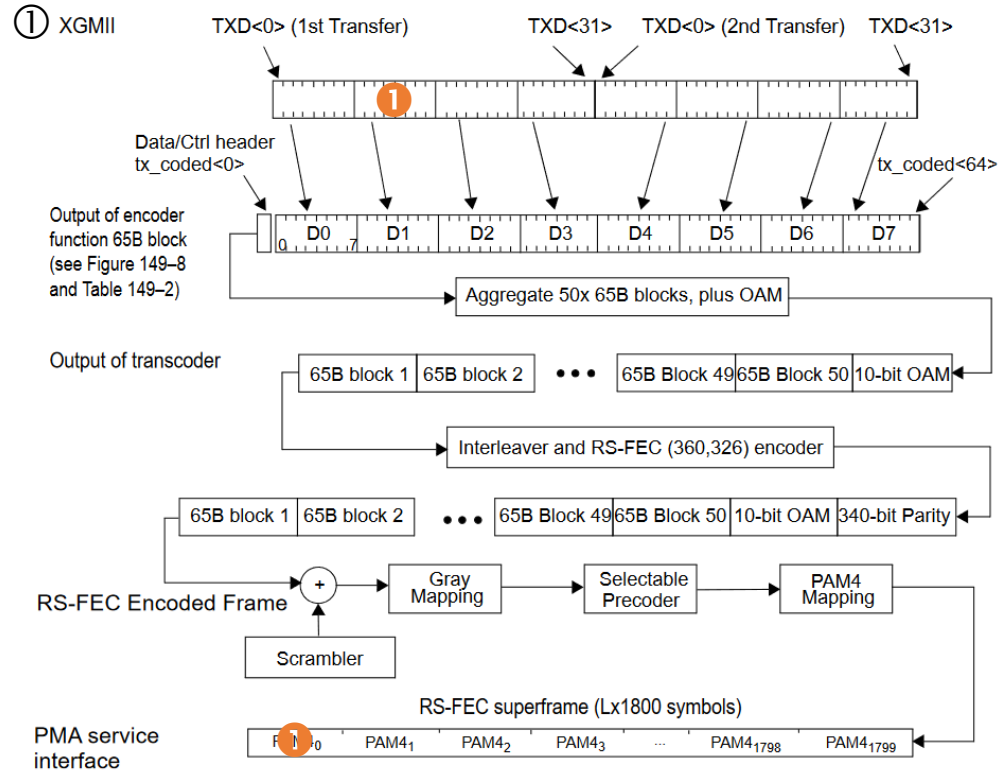
Across the MII ⑩, there are NEVER any IDLE symbols between the Preamble and the FCS!



Below the (g)RS the time between ① and ② is always given by <the number of bits contained in the Ethernet Frame> divided by <the nominal bit-rate of the MII ⑩>



PHY Delay



NOTE 1—This figure shows the mapping from the XGMII to a 64B/65B block for a block containing eight data characters.

NOTE 2—Figure shown for L = 1.

Figure 149-6—PCS Transmit bit ordering

continuous bit stream, i.e this could be IDLE symbols or Packet bits

The (maximum) time it takes for any bit within the data stream (here - as an example - the end of the SFD) to pass between the MII ① and the MDI ⑨ is referred to as the (maximum) PHY delay

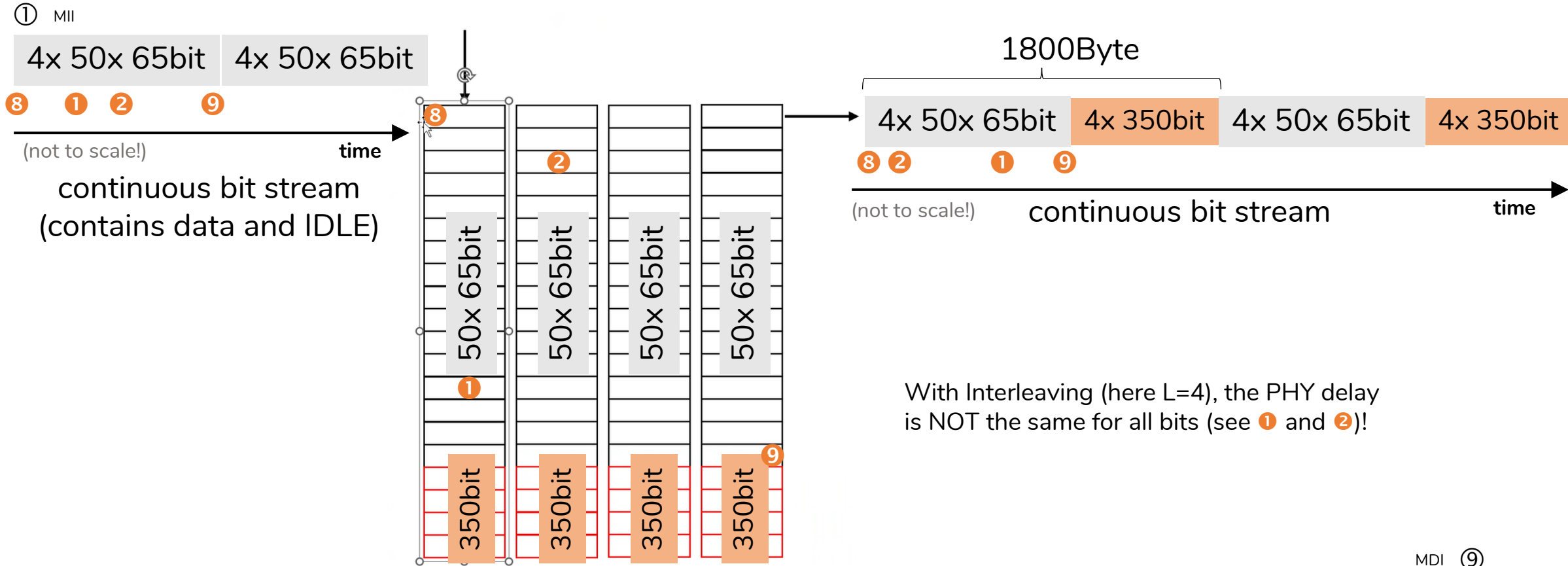
Upper limit values are given in IEEE802.3 Table 149-20

Table 149-20—Delay Limits

Mode	Interleave	Bit times	Pause Quanta	Delay (ns)
2.5GBASE-T1	1x	10 240	20	4096
5GBASE-T1	1x	10 240	20	2048
5GBASE-T1	2x	13 824	27	2764.8
10GBASE-T1	1x	10 240	20	1024
10GBASE-T1	2x	13 824	27	1382.4
10GBASE-T1	4x	20 480	40	2048

⑨ MDI

Interleaving Delay



MDI ⑨

An Attempt at some Definitions

- (maximum) **TX PHY Delay**: Maximum time it takes for any input bit or symbol (⑨) from being available on the xMII (⑩) until it or its equivalent symbol appears at the MDI (⑨)
- **Link Delay**: Maximum time it takes for the SFD (①) to traverse from the MAC PLS (①) of one station to the MAC PLS (①) of the station on the other end of the same link segment
- **Frame Latency**: Maximum time it takes from when the first data bit of an Ethernet Frame becomes available at the MAC service interface (③) of a Talker to when the last data bit of the same Ethernet Frame becomes available at the MAC service interface (③) of a Listener on the other end of the bridged network
- **Image Latency**: Maximum time it takes from when the first pixel of an Image Frame becomes available from the Application (④) of a Camera to when the last pixel of the same Image Frame becomes available at the Application (④) of a Receiver on the other end of the bridged network

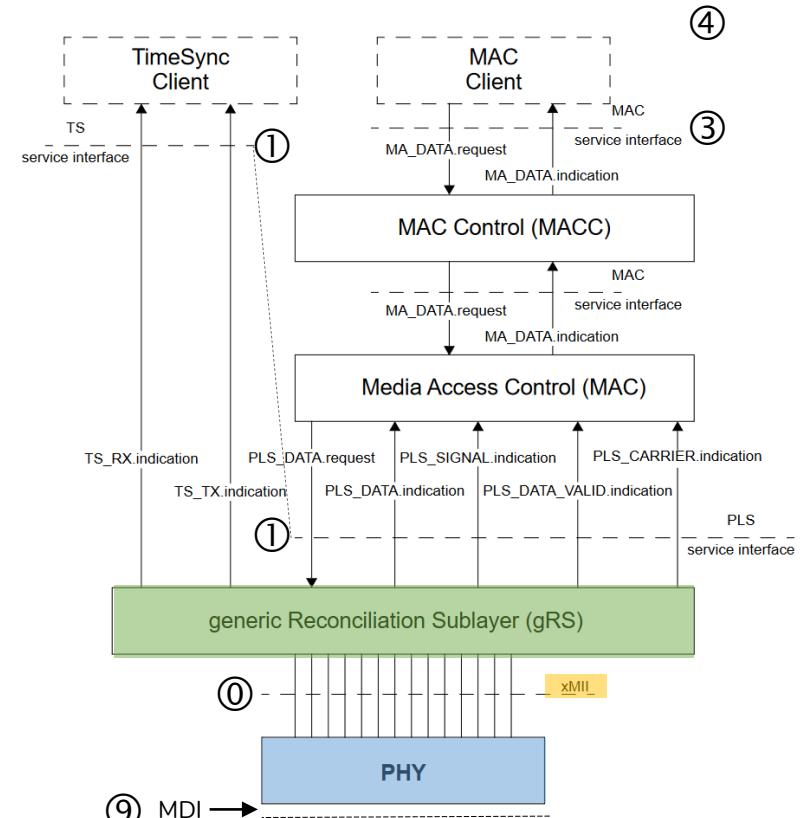
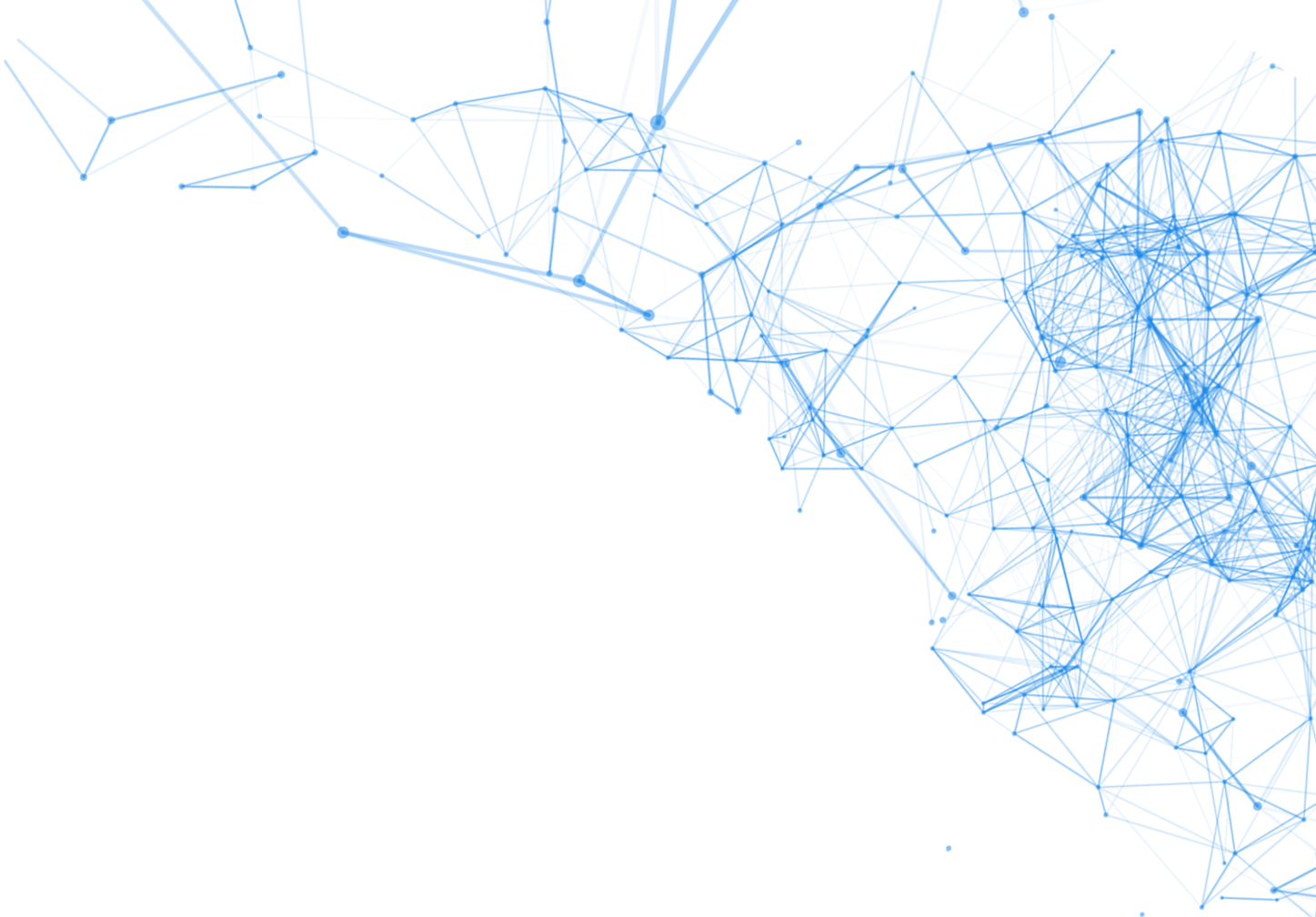



Figure 90-1—Relationship of the TimeSync Client, TSSI and gRS sublayer relative to MAC and MAC Client and associated interfaces



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Contribution to:  **IEEE**

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