Measurements and Simulations on MDI Return Loss including PoC/PoDL

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Presentations considered

- On MDI Return Loss and Power Delivery (Ragnar Jonsson, TJ Houck)
  - MDI Return Loss limit is proposed
  - Not introduce too restrictive requirements for the PoC design
- Power over Coaxial Cable Optimization and Signaling Trade-off (Ahmad Chini, Mehmet Tazebay)
  - Trade-off between signal baud rate and lower part of return loss limit should be observed
- Analysis on PoC inductors in automotive camera applicatios (Jingcong Sun)
  - No inductor with high impedance for frequency more than 3.x GHz in the market
  - Concerns regarding single inductor feasibility

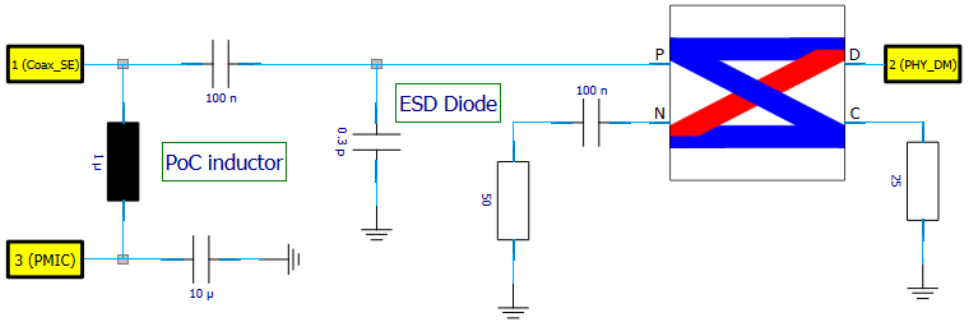
Motivation

- Multiple inductors (2+) are currently used in ADAS cameras PoC circuits.
- If single inductor design is technically feasible at an acceptable return loss limit line, 802.3dm will be very attractive to use.
- Can we find a return loss limit that is (sufficiently) optimal for PoC circuits and PHY design?
- This presentation provides simulation results for RL, and IL, considering realistic PoC circuitry, including parasitic PCB characteristics, to help defining appropriate limit lines. In addition, RL measurements of an actual camera design prototype are provided.

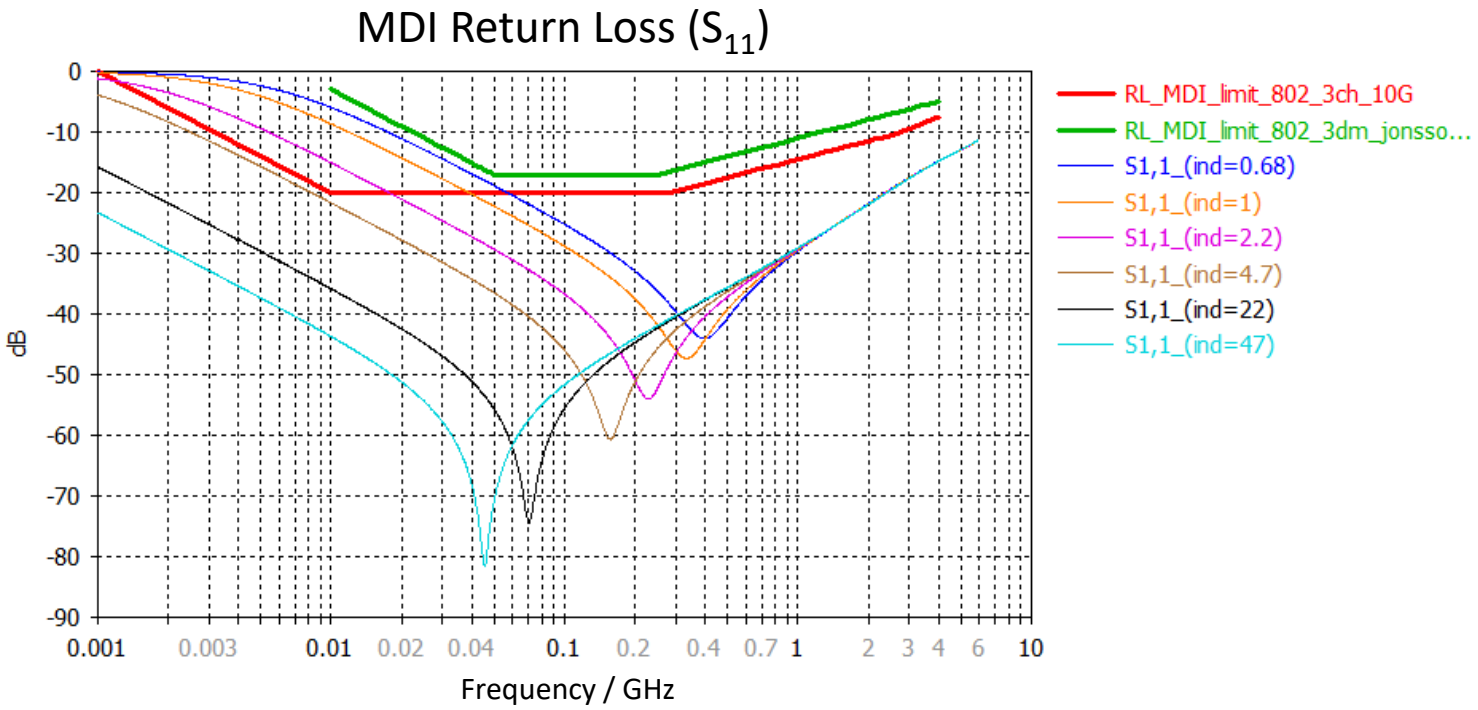
Return Loss Simulation with ideal Inductors on Schematic Level

For ideal inductors:

- Higher inductance improves RL for low frequencies.



Schematic Simulation with ideal Components



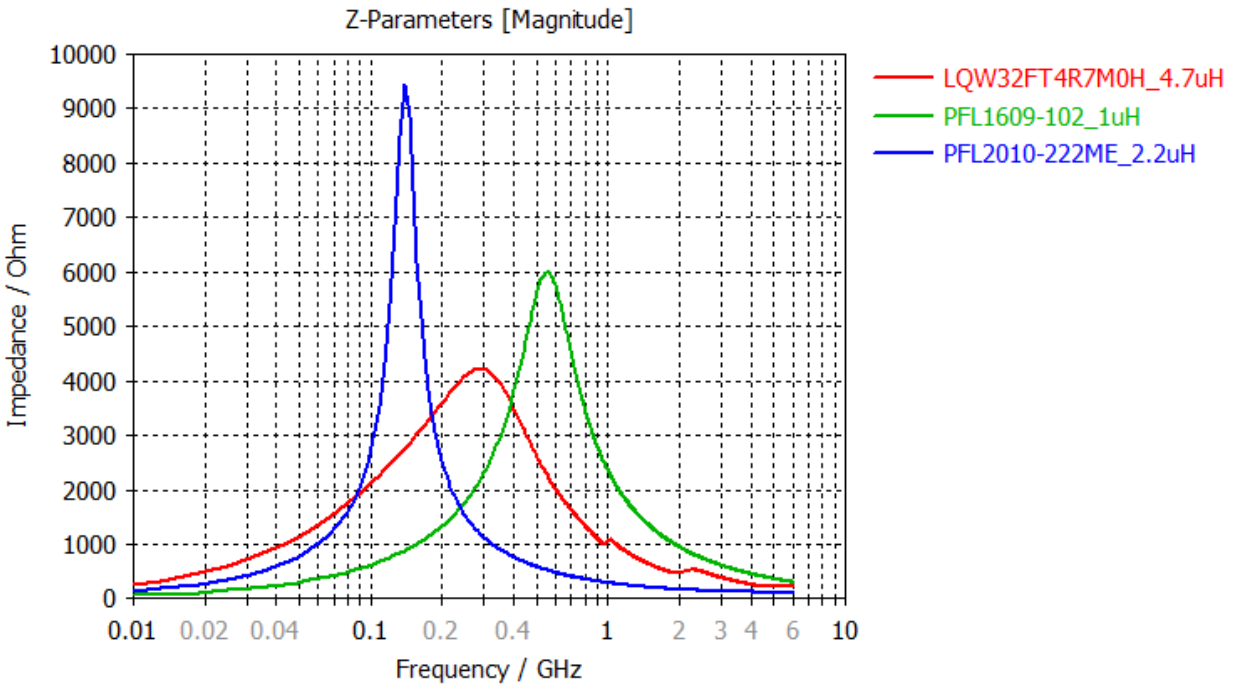
Component Simulation Models used in this Presentation

But in reality:

- Return loss highly depends on parasitic effects, including PCB layout.

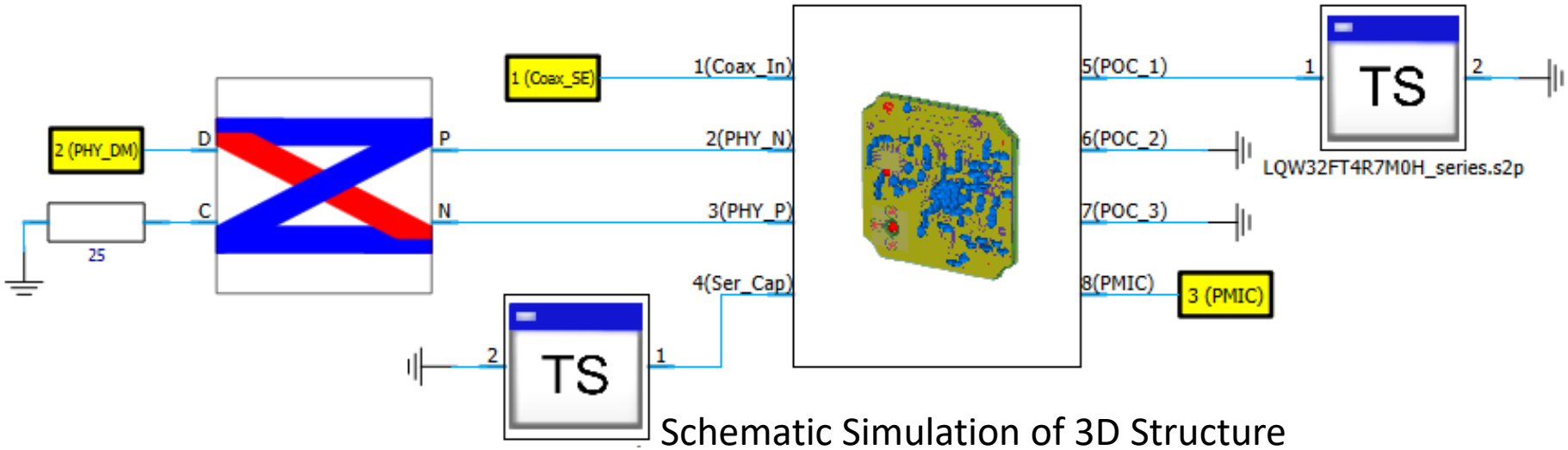
  Following inductors (>500mA) were used for simulations (SPICE / S-parameters publicly available)

  - LQW32FT4R7M0H (4.7uH, 0.28Ω, 1210 SMD)
  - PFL2010-222 (2.2uH, 0.465Ω, ≈0906 SMD)
  - PFL1609-102 (1uH, 0.23Ω, 0603 SMD)
  - Plot shows impedance of each of these inductors

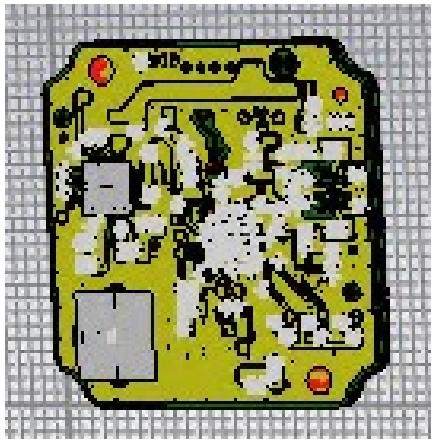


3D PCB Simulation – Setup

- 3D Simulation on return loss of a SerDes prototype PCB
  - Differential-mode PHY
  - Single-ended signaling for the channel (coax)
  - Assembly option up to 3 PoC inductors, but only 1 used
  - Port 3 (PMIC) includes 2x 10uF input capacitors
  - Not included yet: ESD diode, adds ≈ 0.3-0.5pF



Schematic Simulation of 3D Structure



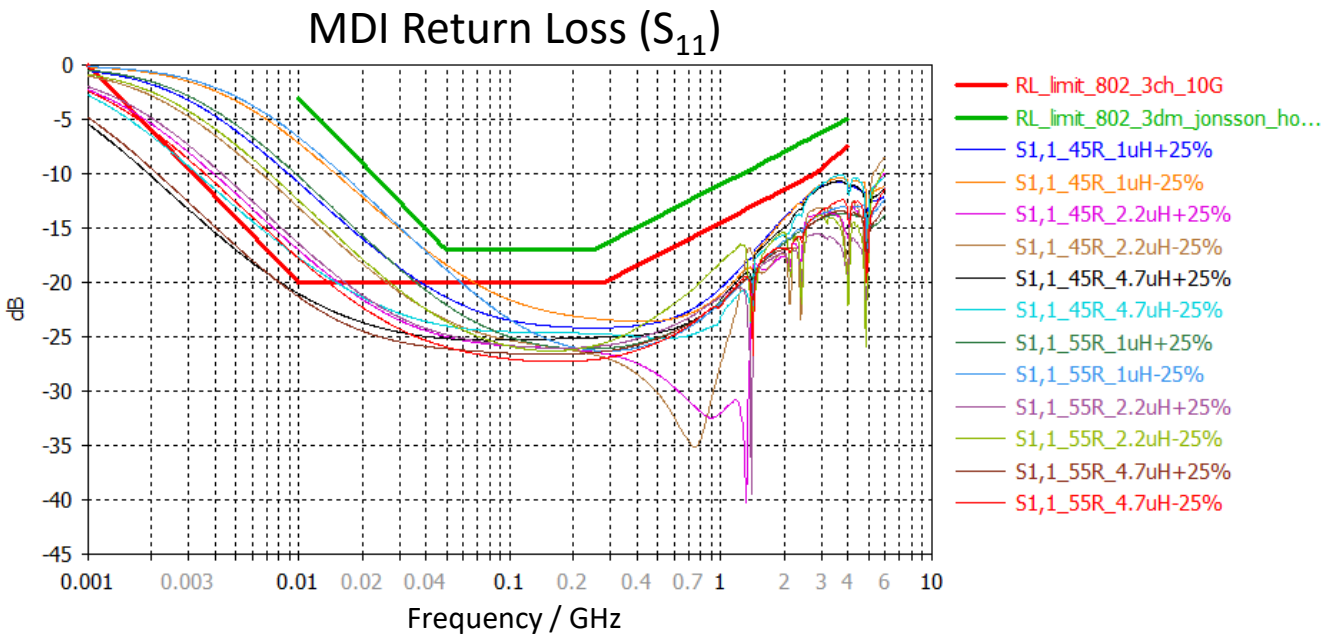
3D PCB View

note: ground symbols connect to respective port reference, there is no global ground.

3D PCB Simulation – Return Loss Results

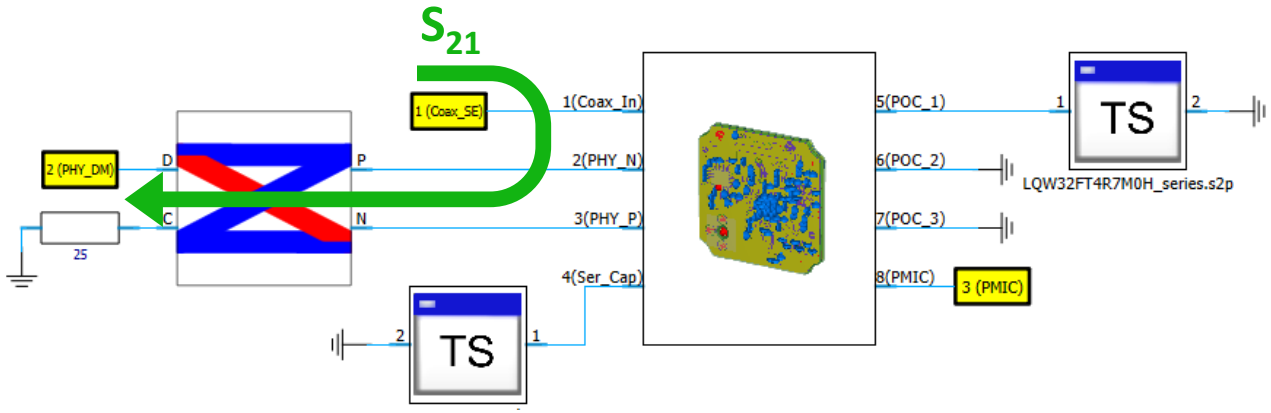
- Considering following imperfections
  - PHY termination (±10%)
  - Inductance tolerance/derating (±25%)
- Plot shows corner cases
- RL for lower inductance (-25%) is worse at low frequencies.

- No violations for proposed limit line jonsson_houck_3dm_02_07_15_24.
- Not even 4.7uH (-25% tolerance/derating) inductors would pass 802.3ch 10G limit.

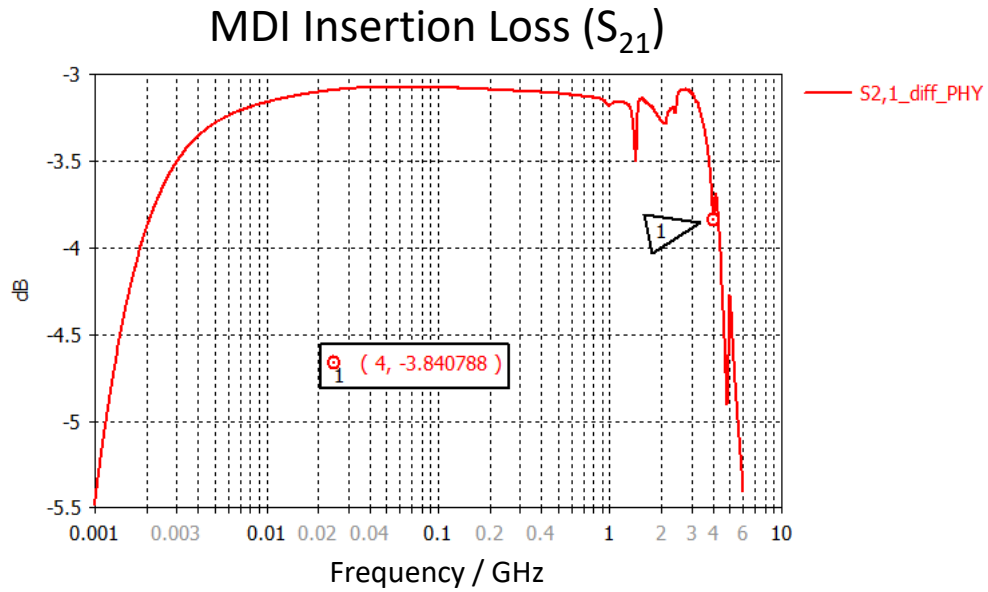


3D PCB Simulation – Insertion Loss Results

- From coax connector to differential PHY
- Including differential-to-single-ended loss
- MDI circuit equals potential 802.3dm implementation including PoC (4.7uH)
- ➢ Insertion Loss drops to ≈ -3.8dB @ 4GHz



Schematic Simulation of 3D Structure



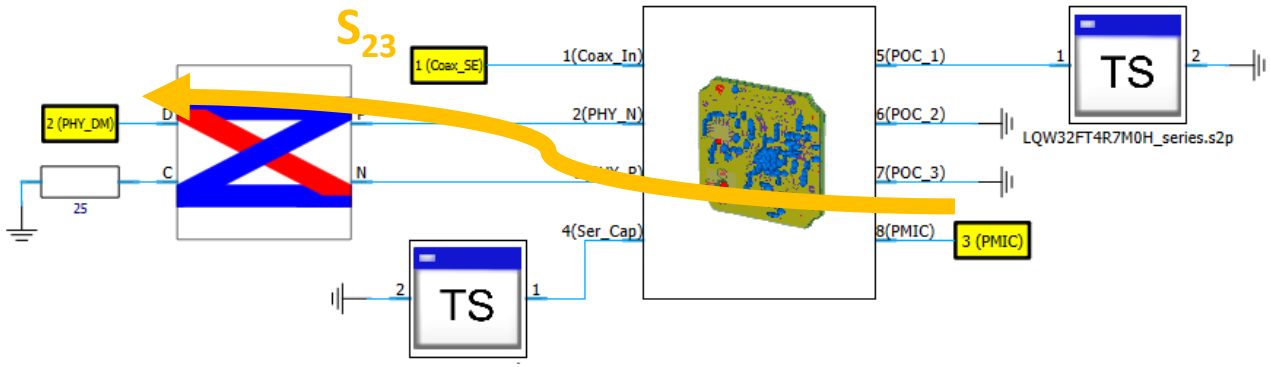
Coupling between PMIC and PHY

- Coupling in simulation depends on the impedance of port 3 (PMIC)

  … what is the output/input impedance of a PMIC?

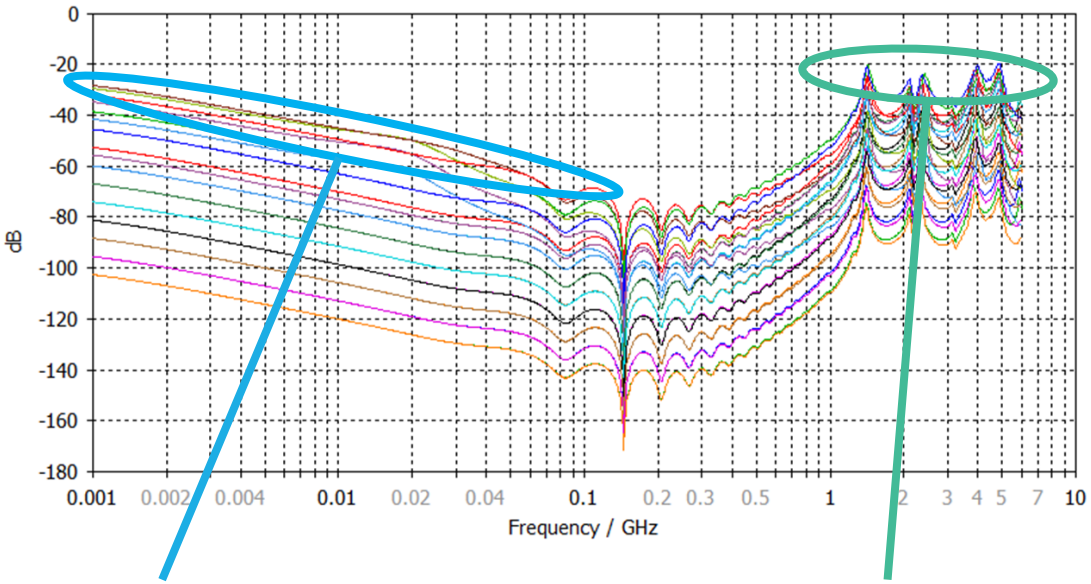
- To get a first estimation, a parameter sweep is done
  - Inductor: 4.7uH

➢ Plot shows a parameter sweep (Z_{PMIC}=1mΩ…100Ω)



Schematic Simulation of 3D Structure

Coupling parameter sweep between PMIC and PHY (S_{23})

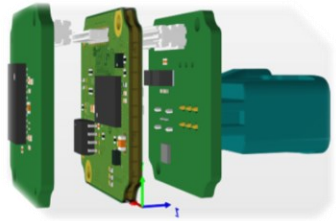


Z_{PMIC} ≈ 100mΩ

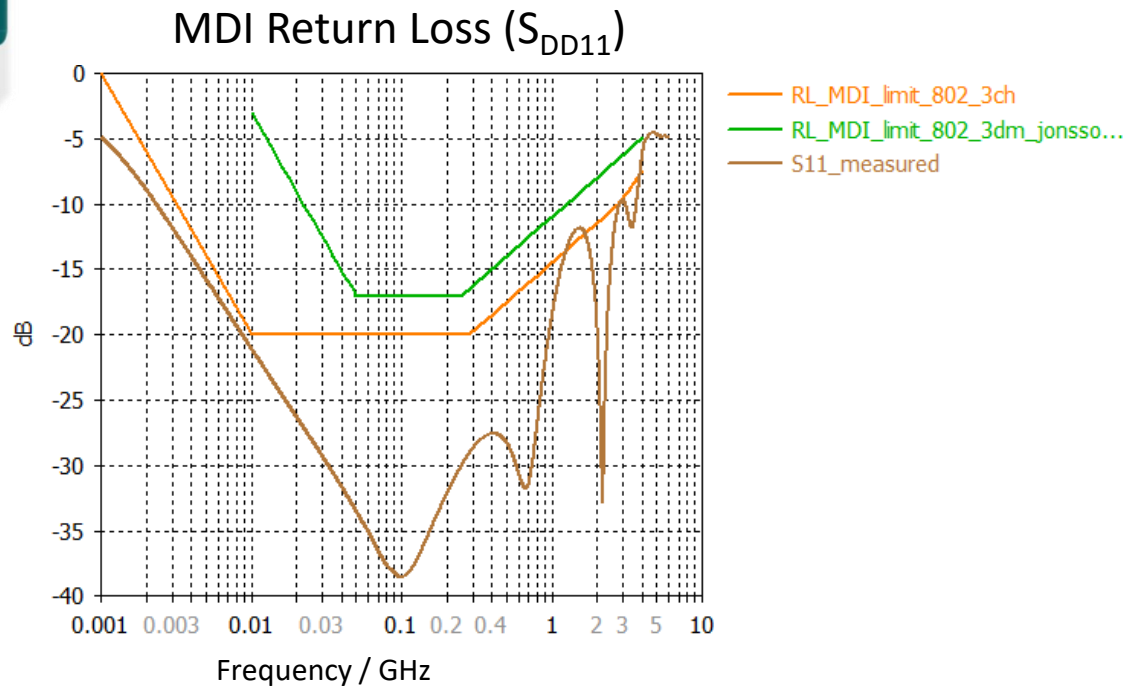
Z_{PMIC} ≈ 10Ω

802.3ch PoDL Return Loss Measurement

- Measured camera prototype (3 PCB design), Ethernet MDI on 2 PCBs.
- Components included
  - Differential automotive connector
  - ESD protection
  - 2x 4.7uH PoDL inductors (without current)
  - Board-to-board connector
  - 802.3ch PHY



Camera Prototype



➢There are some violations for the 802.3ch 10G limit line but can pass the limit line proposed in jonsson_houck_3dm_02_07_15_24.

Conclusion

- The prototype measurement shows that PoDL (and therefore also PoC) single inductor designs are feasible with the return loss limit proposed by Ragnar Jonsson & TJ Houck. (jonsson_houck_3dm_02_07_15_24).
  - 3D simulations of MDI RL show that different PoC inductors would work well with this limit.
  - The high frequency MDI RL limit includes a reasonable margin.

- Low frequencies are matching very well for simulation and measurement.

- The low frequency MDI RL limit could be a bit more relaxed if we limit the lowest supported inductance (e.g., L ≥ 2.2uH) if there is any benefit for PHY implementation.

Thank You!

Backup Slides

PoDL Return Loss can be compared to PoC Return Loss

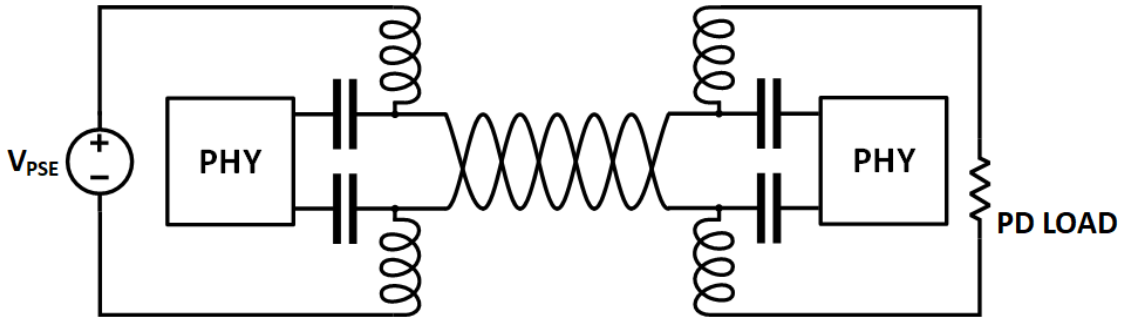
Return loss is defined

$$RL\ (\mathrm{dB}) = 10\log_{10}\frac{P_i}{P_r}$$

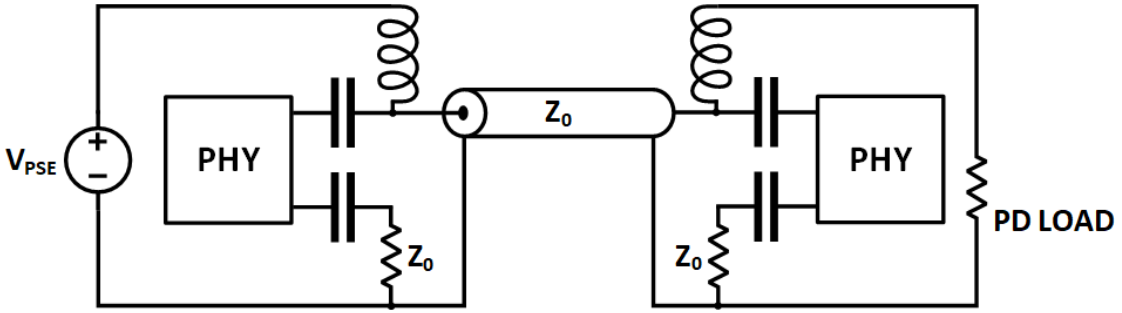
where *RL*(dB) is the return loss in dB, P_i is the incident power and P_r is the reflected power.

Power over Coax (PoC) is basically half the Power over Data Lines (PoDL) circuit for the power injection interface.

Differential return loss measurements for 802.3ch can be directly compared to single-ended return loss for 802.3dm PoC implementations.



Power over Data Lines (PoDL)



Power over Coax (PoC)