Basic Objectives

1. Define a scalable logical **interface** ~~framework~~ that can support arbitrary port speeds and counts while retaining as many of the feature in our Feature Objectives as possible.
2. Define a first electrical interface to provide connectivity to a **single** Ethernet port with 8 or fewer pins operating at line speeds up to 100 Mb/s.
    1. Provide **single** port connectivity without ~~a SerDes~~ **mandating clock recovery from the data**.
3. Define a second electrical interface to provide connectivity to as many as 8 ports **using 8 or fewer pins**, each with speeds up to 100 Mb/s.
    1. Provide eight-port connectivity with **an interface speed** ~~a SerDes~~ not to exceed 2 Gbps.
4. Do not preclude compatibility between the logical interface and 802.3 PHY types that are specified with GMII or XGMII.

Feature Objectives

1. Provide an optional in-band, **error-checked** MDIO management interface.
2. Support Energy Efficient Ethernet (EEE).
3. Support half-duplex operation.
4. Support Clause 148 PLCA.
5. Support full-duplex operation.
6. Support auto-negotiation (e.g. Clause 28, Clause 98)
7. **Provide an extensible out-of-band communications channel between a MAC and a PHY**

Compatibility Objectives

1. Specify a logical and electrical interface between the Media Access Control (MAC)-Physical Signaling Sublayer (PLS) and the following Physical Coding Sublayers specified in:
    1. Clause 96 (100BASE-T1)
    2. Clause 97 (1000BASE-T1)
    3. Clause 146 (10BASE-T1L)
    4. Clause 147 (10BASE-T1S)
    5. Clause 148 (PLCA)
2. Do not preclude support for other existing PHYs specified in 802.3
3. Do not preclude support for proposed 100BASE-T1L PHYs (P802.3dg - Clause 190).
4. **Do not preclude support for proposed 10BASE-T1M PHYs (P802.3da - Clause 188).**
5. Do not preclude the transmission of PTP timestamps across the interface using in-band data.
6. Do not modify the preamble, thus precluding features that rely on the preamble being passed intact by the MII.

*** Note to Task Force – Consider an objective for EMS compatibility**

POPI Termination Points

Figure 35–2 depicts a schematic view of the Reconciliation sublayer inputs and outputs, and demonstrates that the GMII management interface is controlled by the Station Management entity (STA).

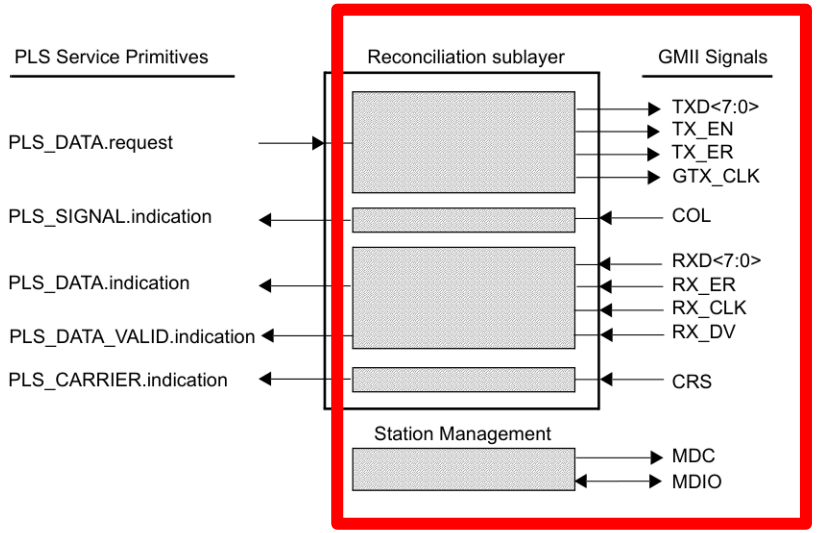

Figure 35–2—Reconciliation Sublayer (RS) inputs and outputs and STA connections to GMII

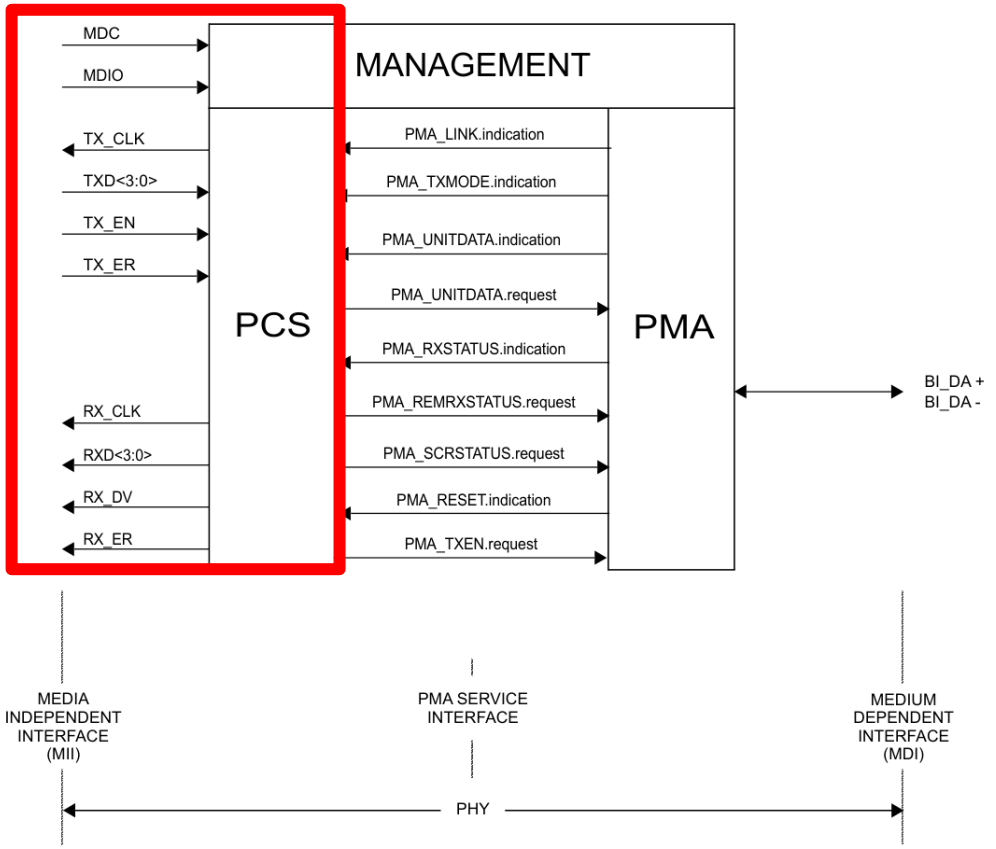

Figure 96–2—100BASE-T1 PHY interfaces