Chip to Module Objectives

Ali Ghiasi - Ghiasi Quantum/Marvell

Chris Cole – Coherent

Karl Muth – Broadcom

Mike Dudek – Marvell

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Background

- **Current 400 GPL objectives are to support 400 Gb/s, 800 Gb/s, and 1.6 Tb/s PMDs/PHYs**
  - Support optional single-lane 400 Gb/s, 800 Gb/s, and 1.6Tb/s Gb/s attachment unit interfaces for chip-to-module and chip-to-chip applications
  - Define a physical layer specification that supports 400 Gb/s, 800 Gb/s, and 1.6Tb/s Gb/s operation over 1 pair of SMF with lengths up to at least 500 m
  - Define a single-lane, two-lanes 400 Gb/s, two-lanes 800 Gb/s, and four-lanes 1.6Tb/s Gb/s PHY for operation over twin-axial copper cables with lengths up to at least 1 meter
  - Define a single-lane 400 Gb/s, two-lanes 800 Gb/s, and four-lanes 1.6Tb/s Gb/s PHY for operation over electrical backplanes
- **This contribution explore adding a C2M short/low-loss specification**
  - In 802.3df a lower loss C2M specification was also explored
    - https://www.ieee802.org/3/df/public/22_11/lusted_3df_03a_2211.pdf.

Straw Polls Related to Lower Loss/NPO C2M in 802.3df

- **There was strong interest to define a lower loss 200G C2M!**

Straw Poll #1

For the front panel pluggable use case, I am interested in 200 Gbps/lane AUI C2M specifications for:

A. medium loss only (e.g. up to ~22 dB IL die-die per lusted_3df_01_220927)
B. higher loss only (e.g. up to ~36 dB IL die-die per lusted_3df_01_220927)
C. both medium and higher loss
D. need more information

pick one

Results: A: 17, B: 11, C: 49, D: 12

https://www.ieee802.org/3/df/public/22_10/motions_3df_221004.pdf

- **There was also strong interest to define a 200G C2M with lower loss for NPO applications!**

Straw Poll #3

I'm interested in 200 Gbps/lane AUI C2M specifications for co-packaged or near-packaged use cases

Y: 54 , N: 10 , A: 22

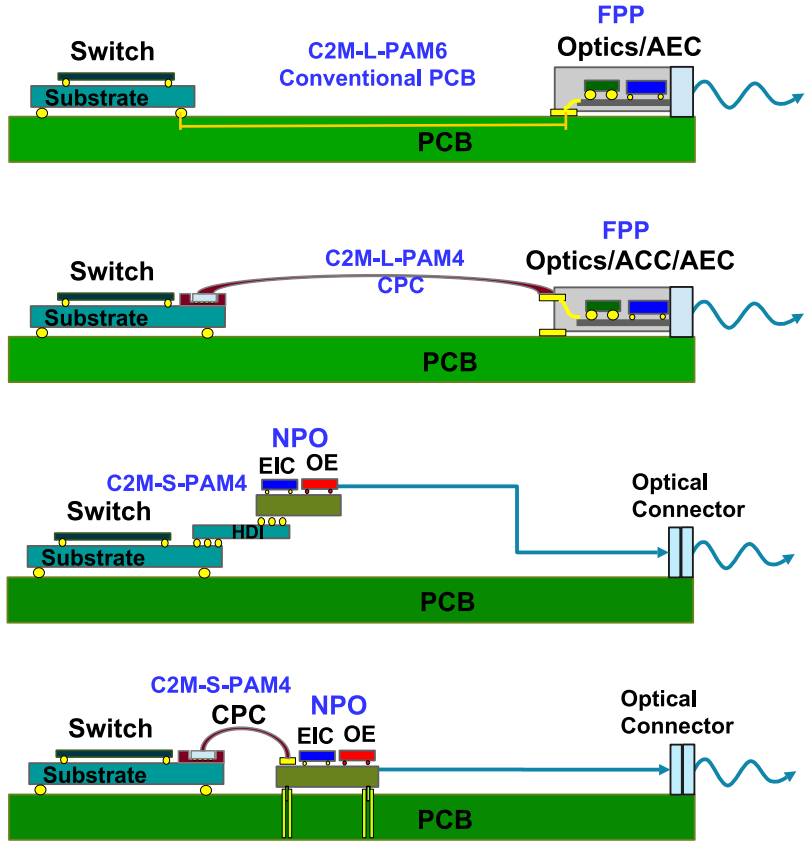
https://www.ieee802.org/3/df/public/22_10/motions_3df_221004.pdf

Merits of Defining C2M-Short

- **C2M-S-PAM4 operates over improved interconnect with lower loss that inherently support PAM4 and include one socket/LGA connector (C2M-S-PAM4 name could be shorten by names such as C2N, C2O, and C2P without the need for PAM4)**

Modulation Parameters	C2M-L-PAM6	C2M-L-PAM4	C2M-S-PAM4
Modulation	PAM6	PAM4	PAM4
Baudrate	~178 GBd*	212.5 GBd	212.5 GBd
Loss @ Nyquist	32 dB	36 dB	20 dB
Pre-FEC BER	~$1x10^{-4}$	$1x10^{-5}$	$1x10^{-5}$
FEC	FEC RS(514, 544)+FECi	FEC RS(514, 544)	FEC RS(514, 544)
Distance	250 mm PCB 500 mm Cable	200 mm PCB 400 mm Cable	100 mm Substrate/CPC
Interconnect	PCB or CPC + 1 FPP connector	CPC + 1 FPP connector	Substrate + 1 socket

* Actual line rate may vary few % depending on the FECi inner code.



FPP – Front Panel Pluggable
NPO - Near package optics

Comparisons C2M-L PM4/PAM6 vs of C2M-S-PAM4

- **C2M-S-PAM expect to offer ~1/2 lower PD than C2M PAM4 – 400G C2M PAM4 equalizer is more like 200G-KR!**

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Modulation	PAM6	PAM4	PAM4
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Transmitter Parameters			
Jitter and rise time	Scaled from 802.3dj	Scaled from 802.3dj	Scaled from 802.3dj
SNR_{TX}	37 dB	33.5 dB	32.5 dB
TX FFE	3pre/2post	3pre/2post	3pre/2post
RLM	97%	95%	95%
Receiver Parameters			
Receiver	6 pre-cursors, 2x4 bank of floating, with Nmax=107, and 1T DFE	6 pre-cursors, 2x4 bank of floating, with Nmax=107, and 1T DFE	5 pre-cursors, 2x4 bank of floating, with Nmax=56, and 1T DFE
Eta0	$5.0x10^{-9}$ V^2/GHz	$5.0x10^{-9}$ V^2/GHz	$7.5x10^{-9}$ V^2/GHz
ENOB	6.5 bits	6.0 bits	5.5 bits
MLSD	On	On	Off

* Actual line rate may vary few % depending on the FECi inner code.

Why Define C2M-Short Now?

- **There was no benefit defining a lower loss C2M interface that used the same OSFP/QSFP-DD connectors and standard IEEE 802.3dj package model due to reflections**
  - For representative 802.3dj C2M channel the worst-case COM are:
    - In case of of low loss channels (<~20 dB) COM limited by ***reflections***
    - In case of high loss channels (>~30 dB) COM limited by ***SNR***
- **During 802.3df/dj development NPO was not as mature a technology**
  - Low loss OSFP/QSFP-DD channels due to high connector reflections didn't allow significantly simpler equalizer
  - Today development of NPO solutions are prevalent in the industry, below are links to several of these development but the list is not exhaustive
    - CPX MSA, see https://www.opencpxmsa.org
    - OIF 12.8T NPO development, see OIF Press Release
    - Broadcom ICA, see https://drive.google.com/file/d/1vVLpZcGjNApgG4dyp1-PCBq-iqUDIbnW/view
- **NPO channels with lower loss (<~20 dB), with improved reflections, and lower ILD inherently supports PAM4 with simpler lower power SerDes interface**
  - In 802.3dv there is clear merits to define lower loss and power C2M interface!

Expected Power Saving for C2M-S-PAM4

- **Typical 200G high speed SerDes power consumption break down are (see ISSCC 2025 7.1 by E-Hung Chen et. al. and 7.2 by A. Mostafa et. al.)**
  - ADC ~35%
  - DAC ~20%
  - Clocking ~15%
  - DSP/Digital/MLSD on ~30%
- **What drives the power dissipation**
  - ADC power dissipation $\propto fs*10^{(6.02xENOB+1.76)/10}$
  - DAC power dissipation $\propto fs*2^{N}$
  - DSP/Digital $\propto$ fs and DSP complexity
- **Relative PD C2M-S-PAM4 to C2M-L-PAM4**
  - ADC ENOB of 5.5 vs 6.0 ~1/2
  - DAC 7 bit vs 8 bit ~1/2
  - Clocking ~15% ~ same
  - DSP/Digital (no MLSD) ~2/5
- **Assuming similar scaling the expect 400G C2M-S-PAM4 SerDes PD will be ½ the C2M-L-PAM4**
  - C2M-L-PAM6 expect PD would be even higher than C2M-L-PAM4.

Summary

- **In IEEE 802.3df/dj the TF explored defining 2 AUI interfaces one with ~22 dB and one with ~36 dB**
  - It was determined that a C2M loss of 36dB was not necessary for most applications and instead 32dB loss adopted that didn't require MLSD
  - Given that NPO wasn't as prevalent the lower loss channels were based on OSFP/QSFP-DD connectors
  - The low loss channels based on OSFP/QSFP-DD were as challenging as ~32 dB channels due to higher reflections and ILD
  - Given lack of benefit defining lower loss C2M the TF decided to only define a single C2M interface with up to 32 dB loss
- **To improve density and power NPO is now becoming mainstream at 200G and will be even more prevalent at 400G**
  - The NPO channels with lower loss, improved reflection, and lower ILD inherently supports PAM4
  - C2M-S-PAM4 expected PD is ~1/2 of C2M-L-PAM4
- **Considering power and density advantages of NPO with C2M-S-PAM4 to better address Scale-up applications the 802.3dv TF should consider adding C2M-S-PAM4 specification!**

Thank You!