Lower BW Tx in 400G/Lane

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400G Optical Tx Specification

CPO channels

- Previously [1], we proposed that 400GBASE-DR specification accommodate lower BW transmitters that are expected from silicon-photonics based CPO systems.
- A few major concerns were raised:
  - Large DFE tap at reference TDECQ Rx implies a large DFE tap at the link Rx as well and that could lead to error propagation issues
  - Lower BW Tx will degrade link SNR compared to a higher BW designs
  - Is silicon photonics the best option for CPO? Do other technologies (III-V, TFLN …) avoid the low BW issue?

- While other technology or process choices exist, silicon-photonics based CPO have two major advantages:
  - Modulators integrated in the silicon process consume smaller area compared to heterogenous integration
    - Enables high radix integration
  - Lower cost and higher manufacturing capacity of silicon based photonic components:
    - Enables high volume manufacturing at scale

- In this presentation, we aim to address:
  - RS-FEC performance while intentionally taking the DFE tap of an end-end link to extreme value of 1.0 (h1==1.0)
  - Quantify the SNR degradation (with h1==1.0) of a link with E-O BW of 80GHz compared to state-of-the-art BW of 92GHz.

[1] Inclusion of CPO channels in the 400G/lane Optical Specifications

400G Optical Channel

212Gbaud/s, PAM4, FFE + DFE

BT4: 106 GHz
6b ENOB
Tx pre-coding
5-tap TxFIR (2-1-2)

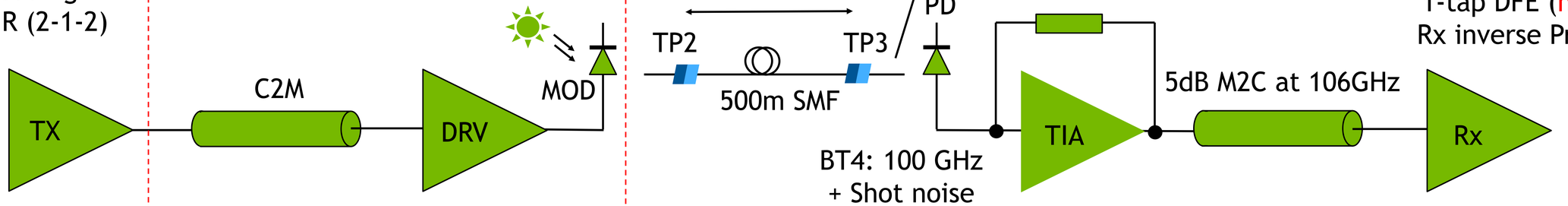
Pavg = <sweep>
CW laser
RIN = -152dBc/Hz
(RIN_OMA= -142dBc/Hz)

ER = 3.0dB
TDECQ= 3.6dB

0-3dB channel loss
(0.5dB MPI loss included)

3dB Rx coupling loss

BT4: 90 GHz, 8nV/sqrt(Hz)*
21 tap FFE (5-1-15)
1-tap DFE (h1==1.0)
Rx inverse Precoding

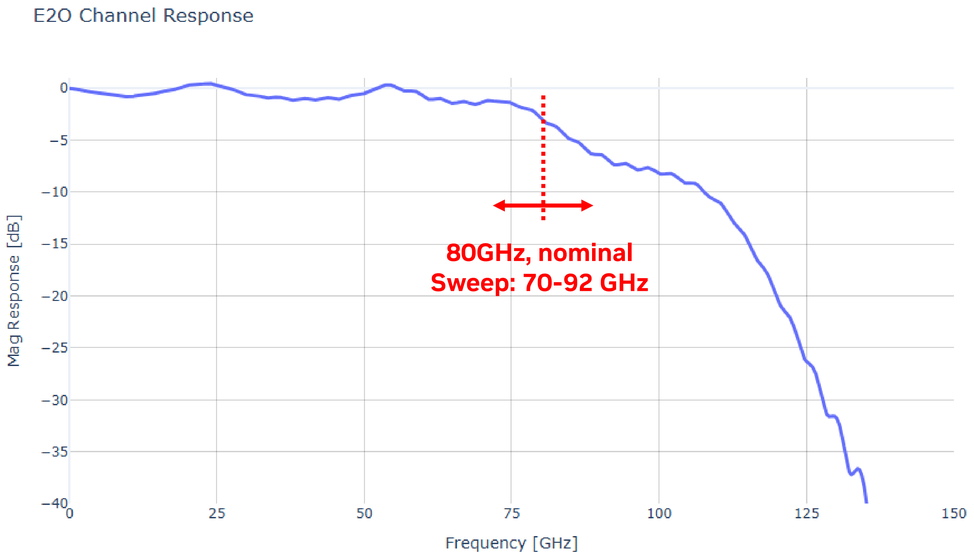


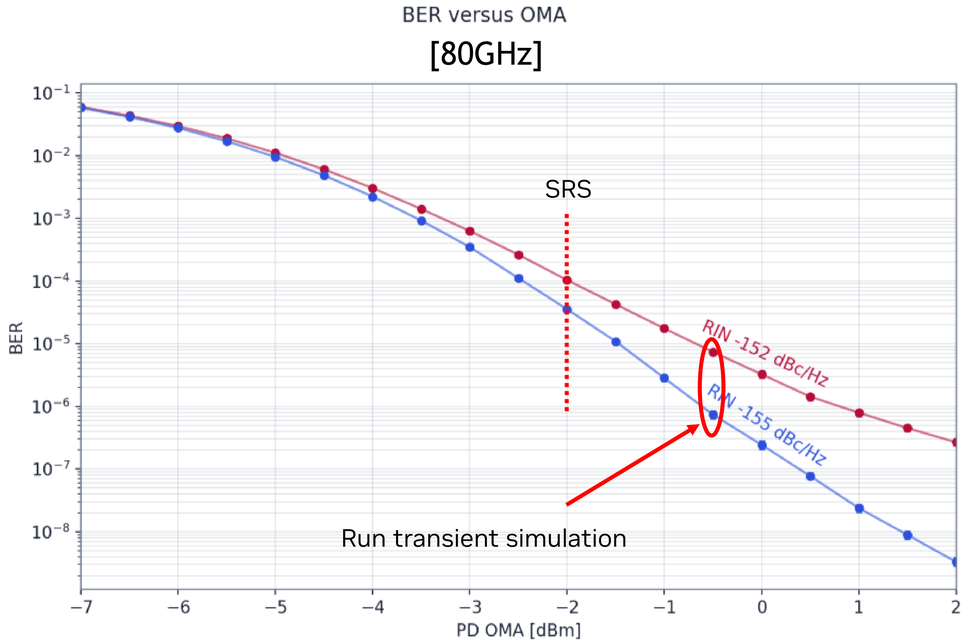
E-O response

BT4: 100 GHz
+ Shot noise
0.9A/W

28 pA/sqrt(Hz)
BT4: 92 GHz

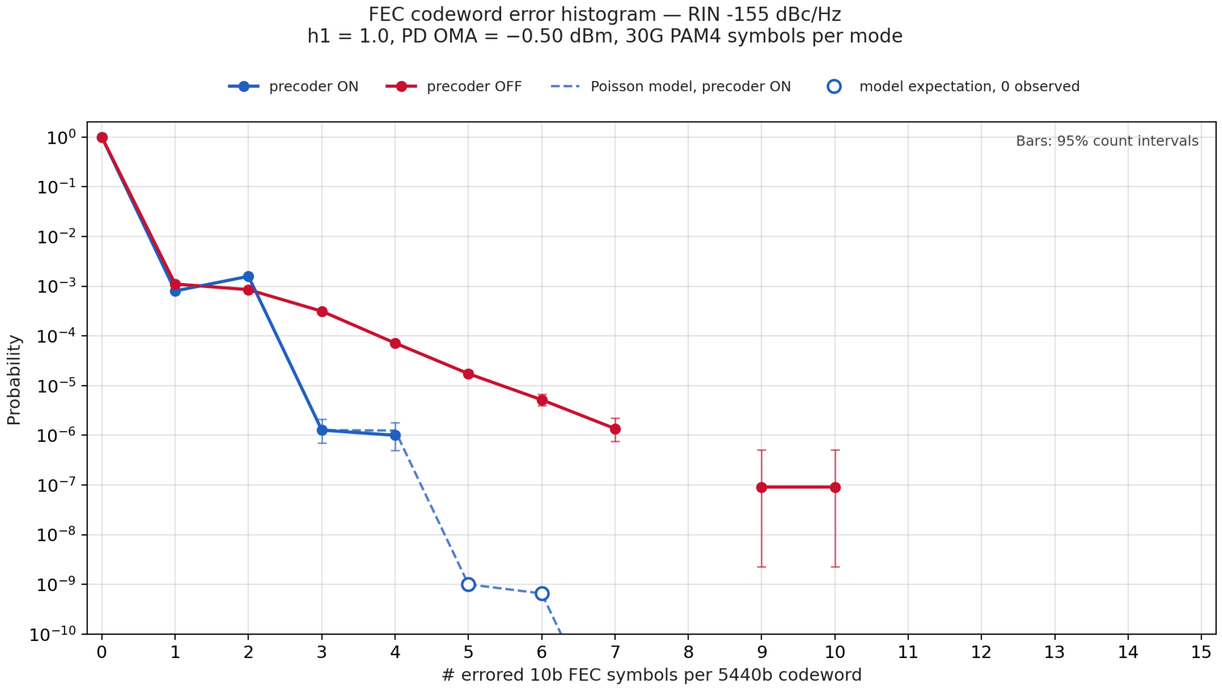
* Rx noise representative of ADC ENOB and AFE noise

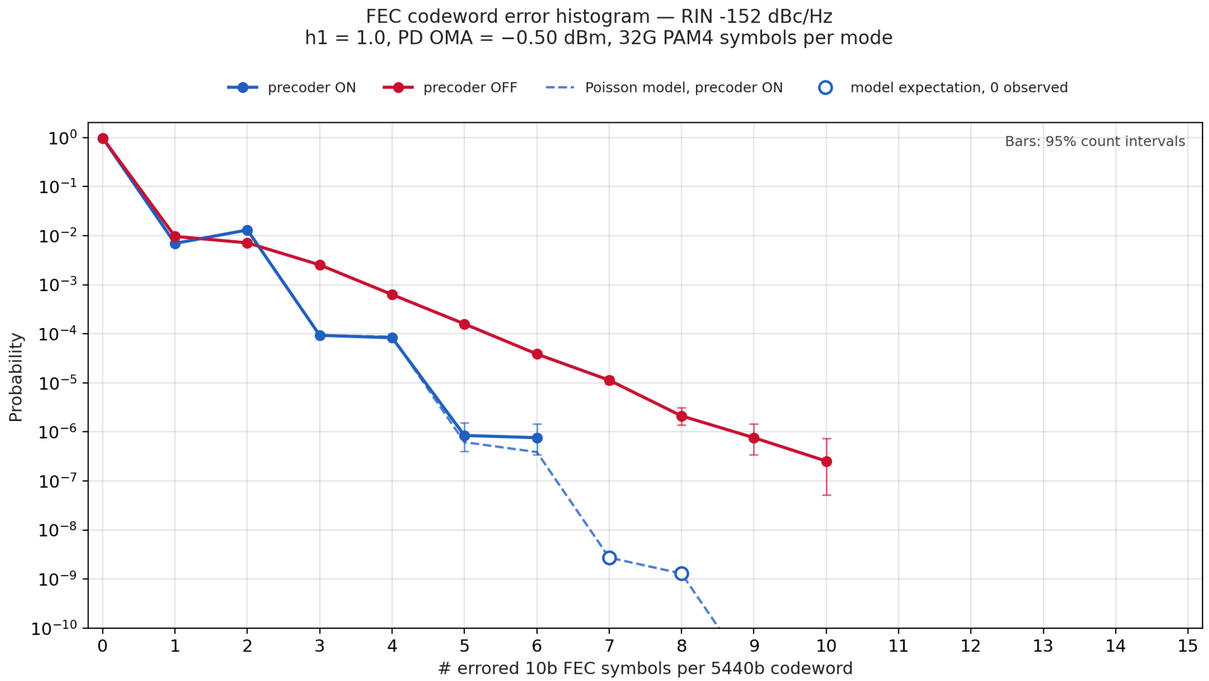




400G Optical Channel

FFE + DFE1 at Rx

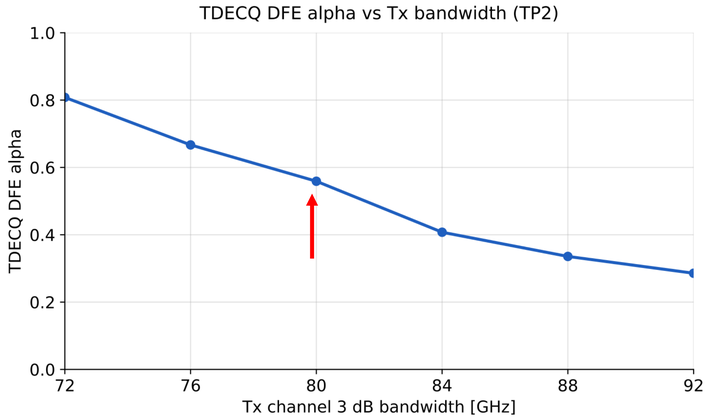


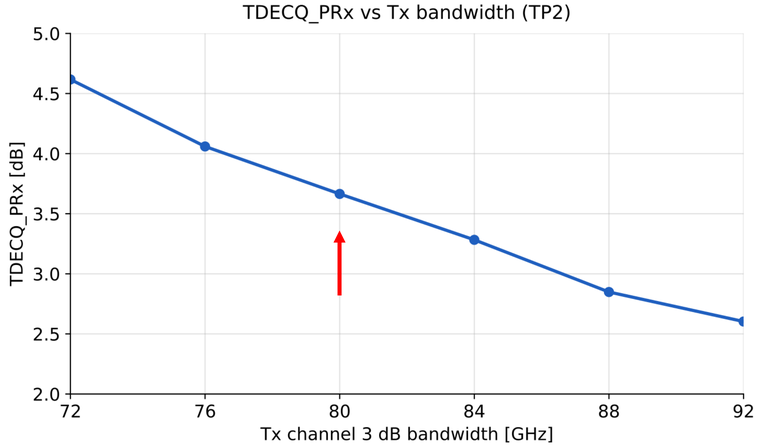


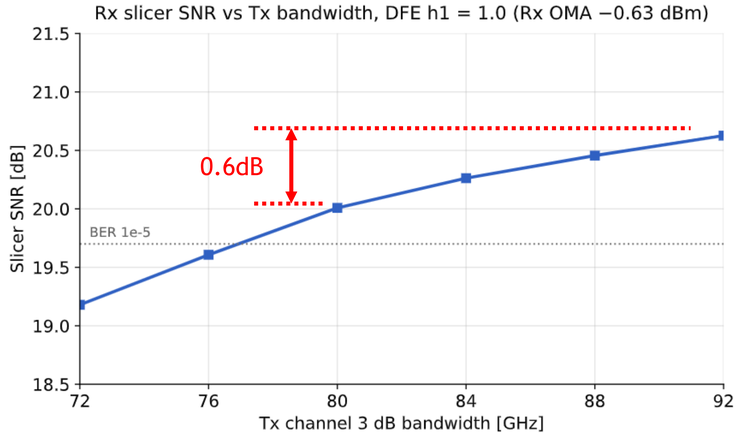
- Precoding is effective in eliminating error bursts even when h1==1.0
- Post-FEC performance is shown with 1-way RSFEC(544,514).
  - 4-way will improve results further.

TDECQ, Alpha, Link SNR vs. BW

Sensitivity to E-O BW at TP2



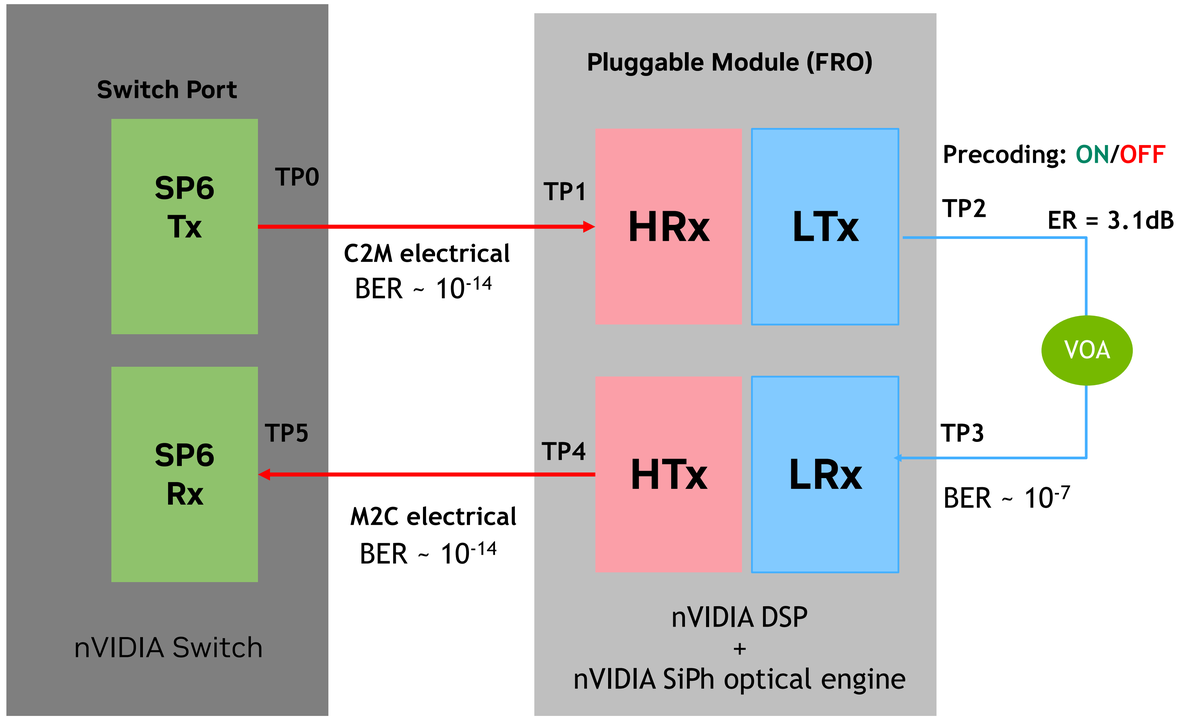


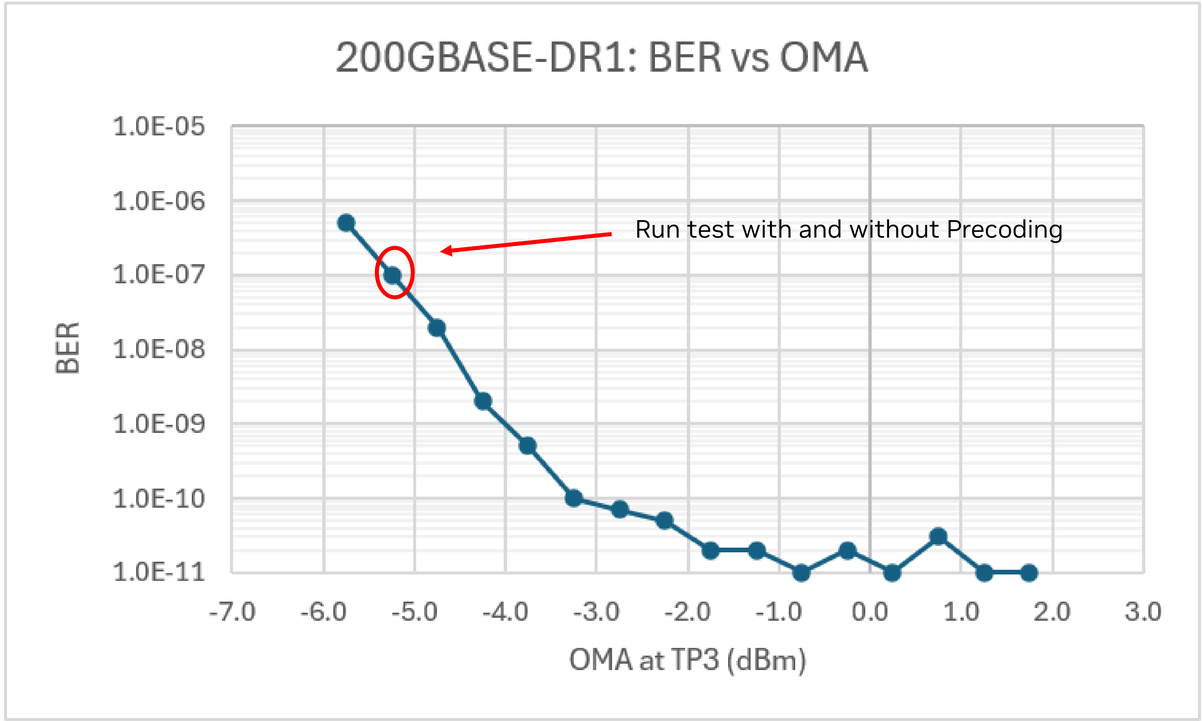


- TDECQ-DFE tap, α, inside [0.4, 0.7] for $\pm$5% BW variation around 80 GHz
- Link SNR penalty of 80GHz BW compared to 92GHz is around 0.6dB

SW+Module: Test setup

200G/lane Line Rx with h1==1.0

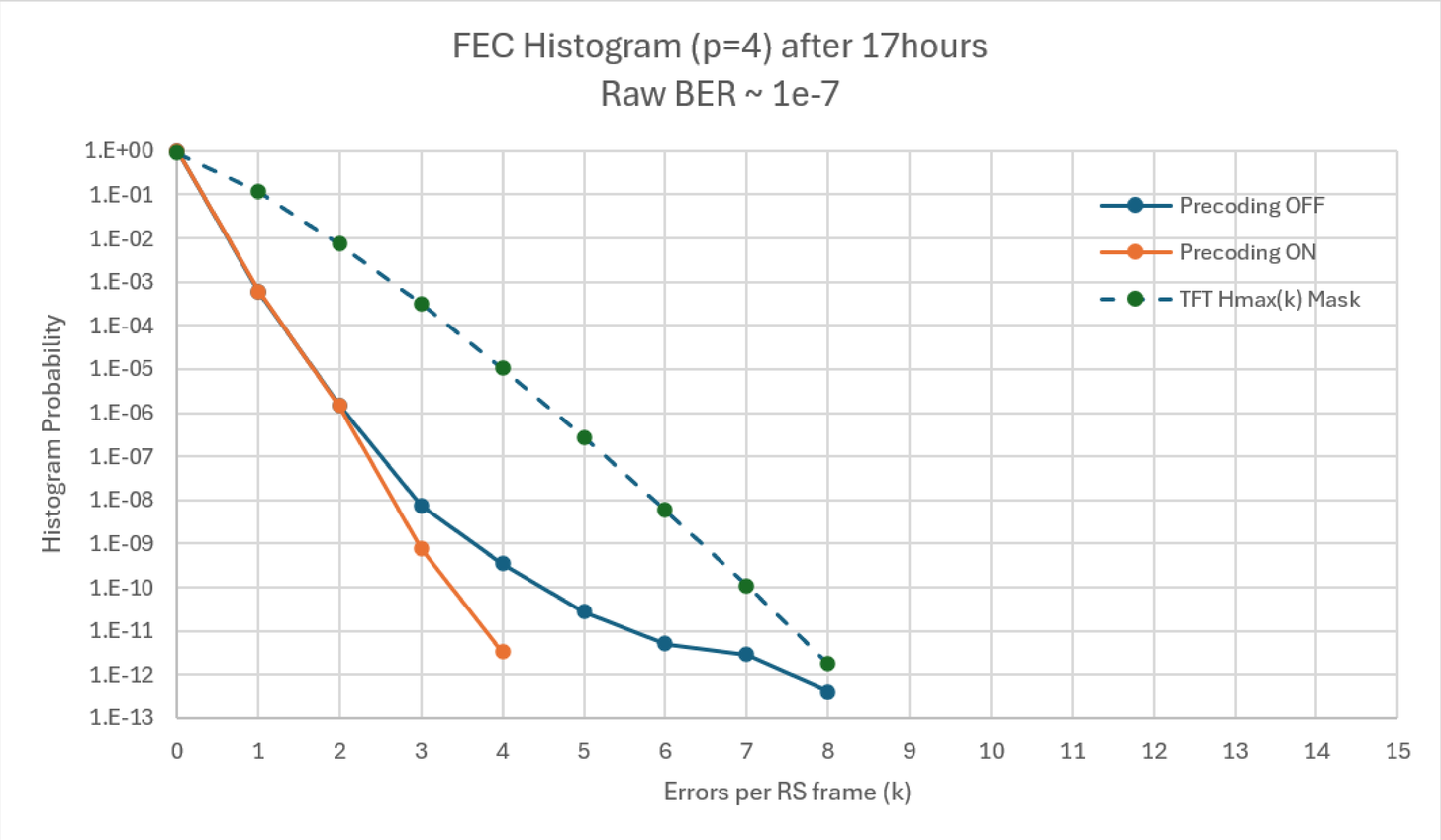




- Adjust Line-side OMA at LRx (using VOA) to operate around Line-side raw BER of 10^{-7} while holding h1==1.0
- Record FEC histograms with and without Line-side Precoding (run time = 17 hours each)

SW+Module: Test setup

200G/lane (802.3dj) Line Rx with h1==1.0



- Precoding is effective in eliminating error bursts
- Note: 802.3dj uses 4-way interleaving (p=4) for RS-FEC

Summary

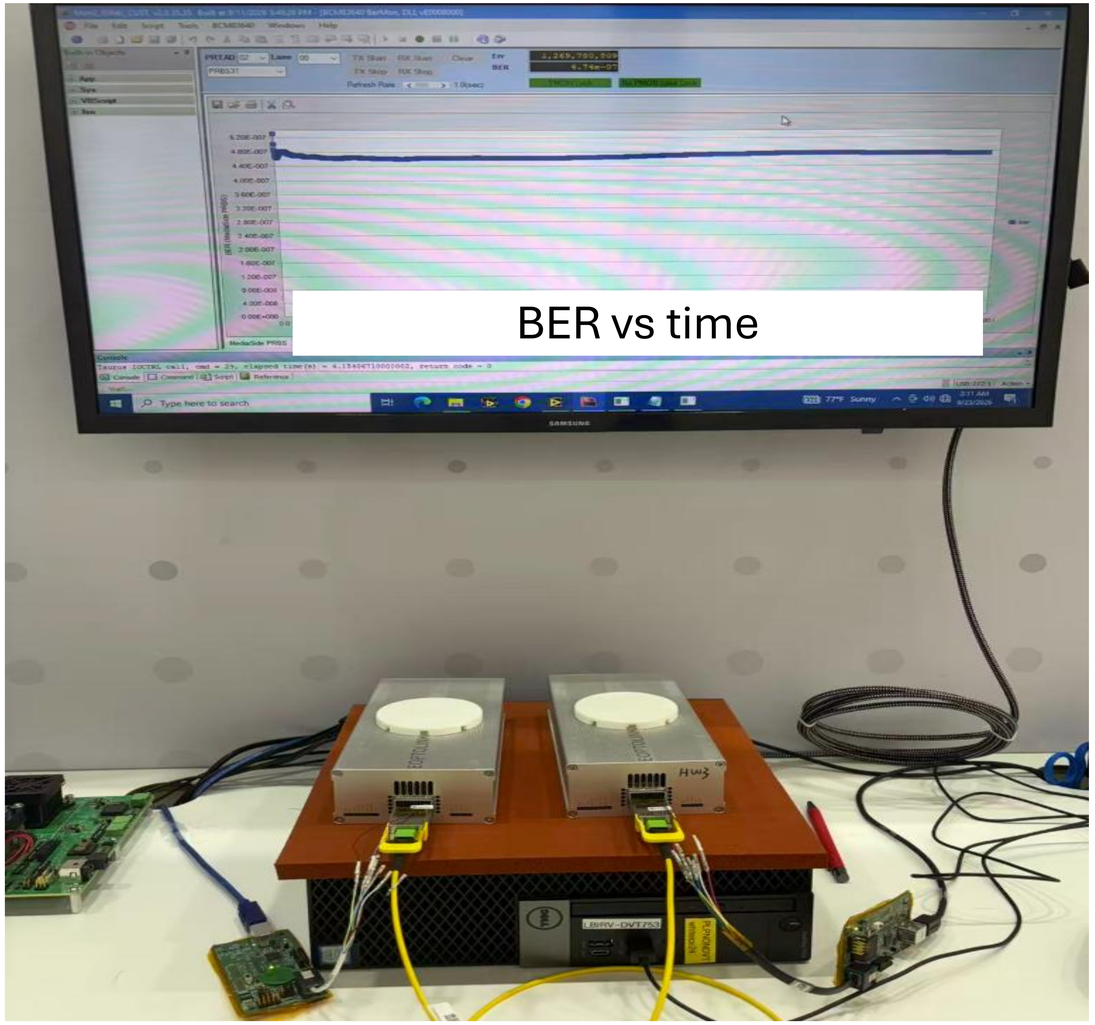
Low Tx BW Optical channels

- A lower BW Tx (with TDECQ=3.75dB and α <= 0.7) can operate with end-end link penalty under 0.6dB compared to a high BW Tx. This seems like an acceptable accommodation for technologies with some intrinsic limitations.
- Differential Precoding (MOD4/[1+D]) mitigates error propagation in the end-end link with high DFE tap (h1=1.0)
- Real lab data from 200G systems with a forced h1=1.0 at the Rx for the end-end link demonstrates the effectiveness of Precoding.
- E2O transfer function will be submitted to 802.3dv channels

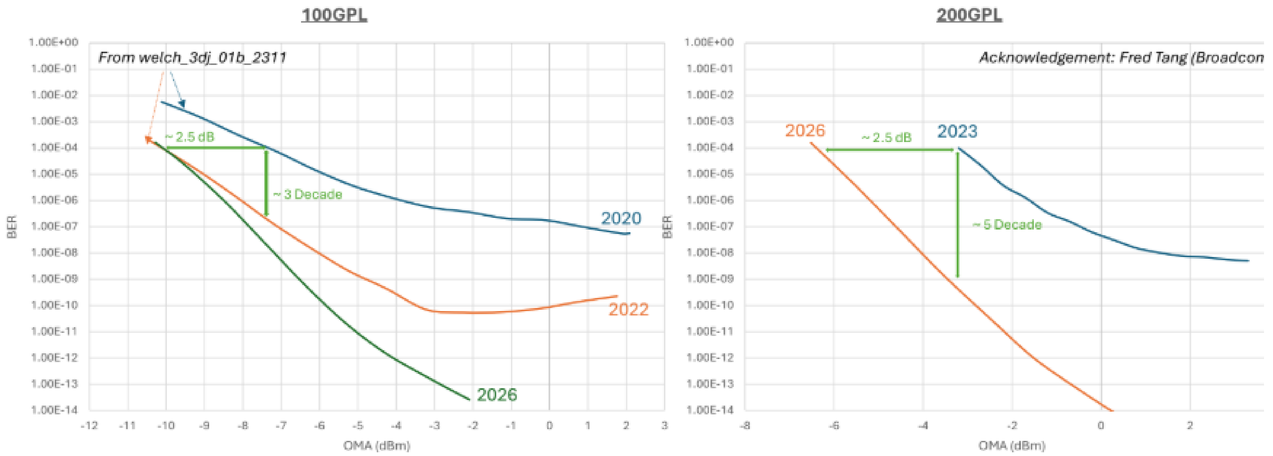
Backup

425 Gbps full module ECOC demo: BER = 4.5 e-7

TIA/PD noise: First generation (>> 20pA/Hz))



Other : Improvements in Time



Each rate generation has seen considerable margin expansion during production ramp

IEEE 802.3 400 Gbps/Lane Signaling Task Force - November 2026 14

- From Brian Welch IEEE 802.3dv Nov 2026, slide 14
- Eco-system improvements in 100/200Gbps expected to continue to 400Gbps

- Shown with: OMA (@TP3) ~3.5dBm, TIA noise >> 20pA/rHz

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