Towards a PMA baseline for 400GbE/800GbE/1.6TbE over 400G/Lane

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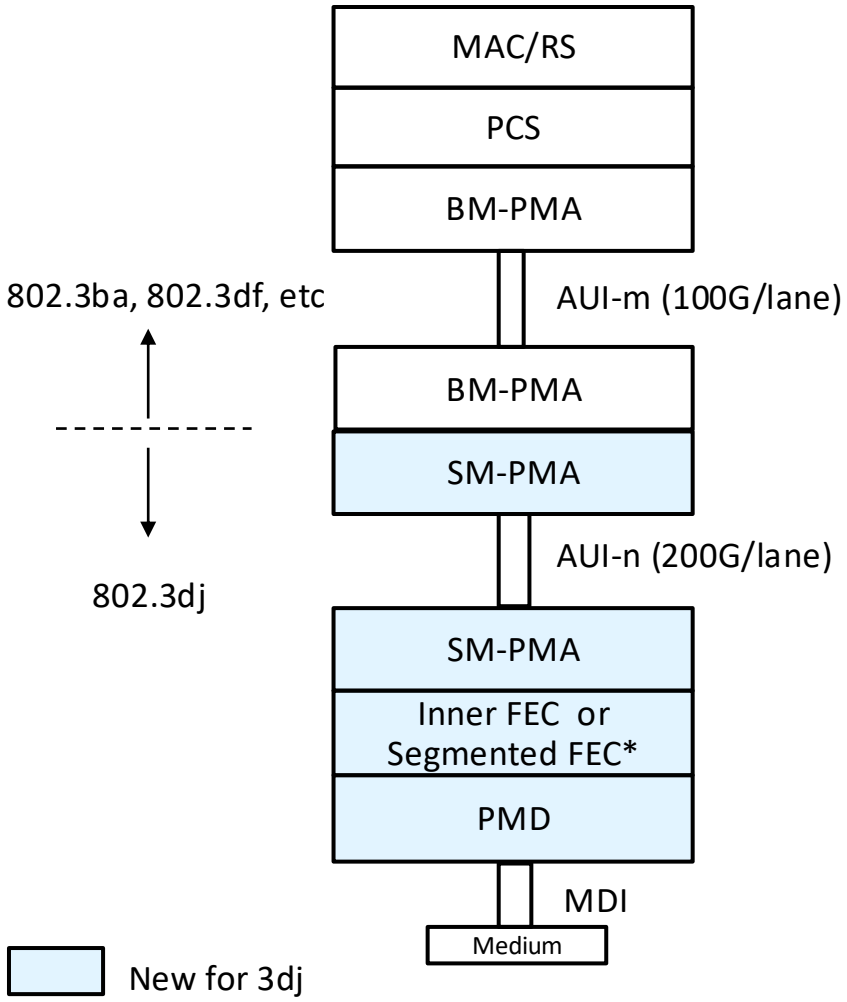
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Outline

- Summary of 802.3dj PMA over 200G/Lane (Clause 176)
- Key considerations in scaling to 400G/Lane
- PMA options for 400G/Lane
  - PCS or 200G PMA lanes to 400G PMA lanes
  - PAM4/PAM6 options
- Summary

P802.3dj Logic Architecture (Review)



*Inner/Segmented FEC conditional on PMD type

SM-PMA

- RS symbol-level multiplexing from PCS lanes to 200G PMA lanes
- Four-way RS-FEC codeword interleaving (of RS symbols) on the 200G PMA lanes
- Improves burst error tolerance
- Note: conversion between bit-muxed 100G lanes and symbol-muxed 200G lanes is achieved via back-to-back BM-PMA and SM-PMA.

Inner FEC or Segmented FEC

- Additional FEC is conditional on PMD type
- Inner FEC can be added “on top” of existing RS-FEC (CL 177, 184)
- Segmented FEC can terminate RS-FEC and add a new FEC (CL 186)

Strong support in September 2026 straw poll to use 802.3dj logic architecture as basis for 802.3dv logic (https://www.ieee802.org/3/400GPL/public/2609/400GPL_Motions_Straw_Polls_2609.pdf)

Summary of 802.3dj PMA over 200G/Lane (Clause 176)

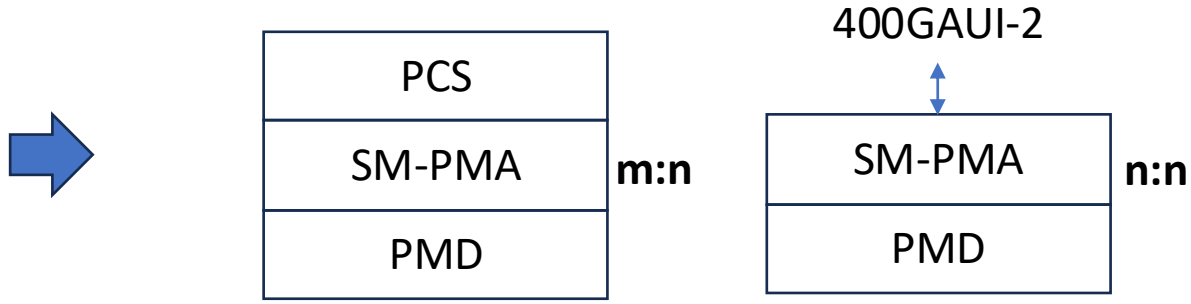
- Symbol Muxing (SM-PMA) for all MAC rates using 200G/lane
  - 800GbE/1.6TbE: RS-FEC Symbol muxing with 4-way CW interleaving on PMA lanes
  - 200GbE/400GbE: Converts from PCS 2-way CW interleaving to 4-way CW interleaving and Symbol muxing on PMA lanes

- Three types of SM-PMA:
  - m:n PMA : PCS lanes to 200G PMA lanes
  - n:m PMA : 200G PMA lanes to PCS lanes
  - n:n PMA : 200G/Lane to 200G /Lane

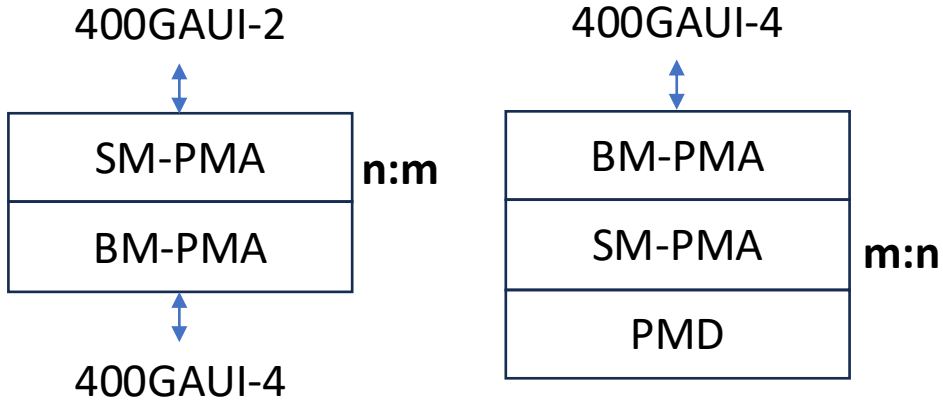
- PAM4 symbols or “stream of bits” options for all 200G/lane interfaces
  - Example: PMA interface to an Inner FEC is “stream of bits”

802.3dj PMA sublayer usage & stack-up examples

- SM-PMA basic uses
  - PCS lanes to 200G lanes
  - 200G lanes to 200G lanes



- SM-PMA stacked with BM-PMA for lane speed conversion
  - 200G/lane to 100G/lane
  - 200G/lane to 50G/lane
  - SM-PMA to/from BM-PMA connection uses PCS lanes



- Refer to Annex 176B to see all PMA stack-up options

SM-PMA : Symbol-muxed PMA (CL 176)
BM-PMA : Bit-muxed PMA (CL 120, 173)

Key considerations in scaling to 400G/Lane PMA

- Keep symbol muxing behavior (same as 802.3dj)
  - Symbol mux from PCS to PMA lanes with 4-CW interleaving for all port speeds

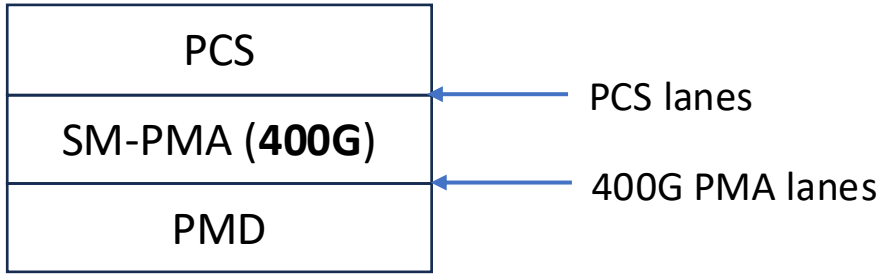
- Options for creating 400G per PMA Lane
  - **Option A :** PCS Lanes to 400G PMA lanes – like 802.3dj but higher muxing ratio
    - For 400GbE: 16:1 PMA (802.3dj was 16:2 PMA)
  - **Option B :** 200G PMA lanes to 400G PMA lanes
    - For 400GbE: Stack 16:2 PMA (802.3dj Cl 176) and a new 2:1 PMA (802.3dv)
  - Both options for specification description only and do not change observable functionality

- Options to handle PAM4 and PAM6 encoding
  - **Option 1** : Include both PAM4 and PAM6 options in the PMA and/or Inner FEC sublayers
    - Following precedent from 802.3dj
  - **Option 2** : Move PAM4 and PAM6 coding options to separate sublayers (not in SM-PMA)
    - PMA becomes purely muxing logic (PCS lanes to “400G streams of bits”)
    - PAMx coding defined outside and used as needed (“400G streams of bits” to PAMx)
  - Both options for specification description only and do not change observable functionality

Options A&B for PCS to 400G PMA Lanes

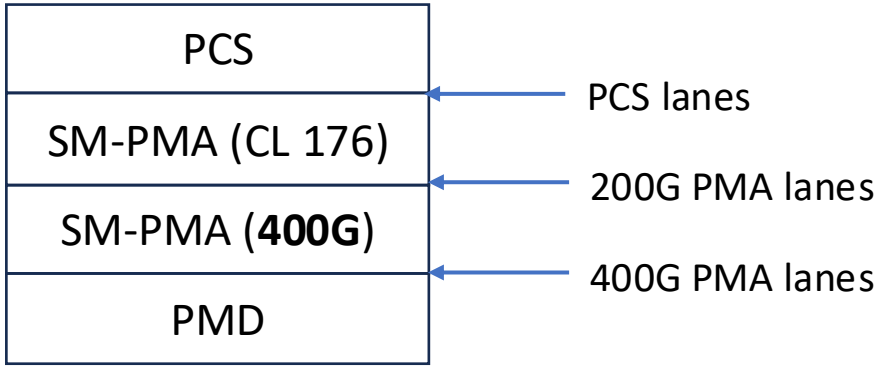
A: Direct PCS to 400G PMA lanes

- Similar to Clause 176 SM-PMA
  - 2x higher muxing ratio
    - For 400GbE: 16:1 PMA (was 16:2)
    - For 800GbE: 32:2 PMA (was 32:4)
    - For 1.6TbE: 16:4 PMA (was 16:8)



B: 200G PMA to 400G PMA lanes

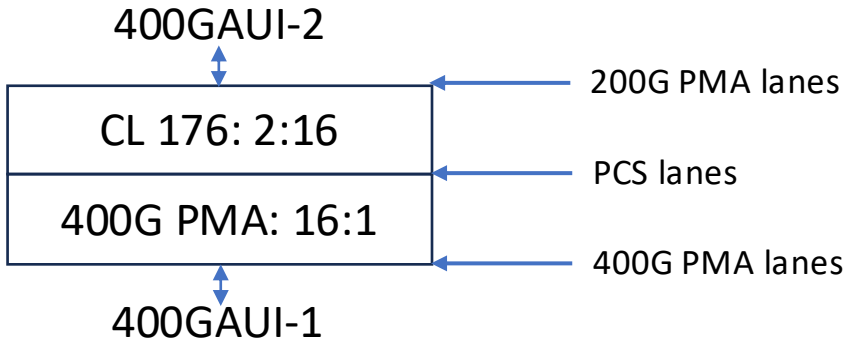
- Stack with Clause 176 (200G-to-400G)
  - Common 2-to-1 muxing ratio
    - For 400GbE: 2:1 PMA
    - For 800GbE: 4:2 PMA
    - For 1.6TbE: 8:4 PMA

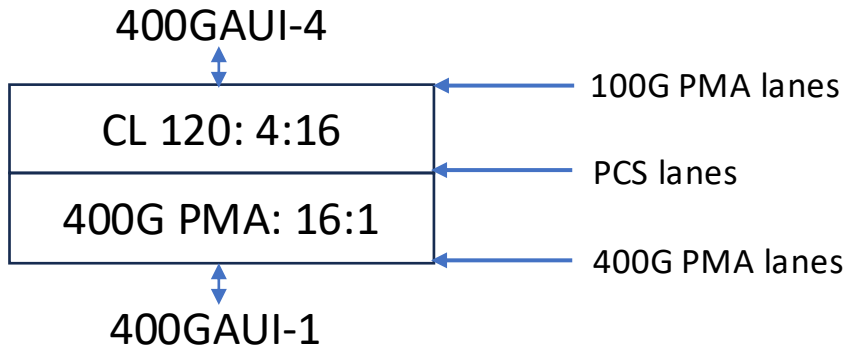


Options A&B for 100G/200G to 400G AUI lanes

A: Direct PCS to 400G PMA lanes

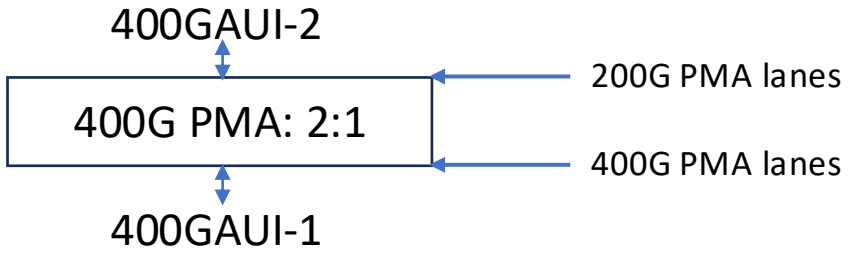
- Back-to-Back PMAs (400GbE)

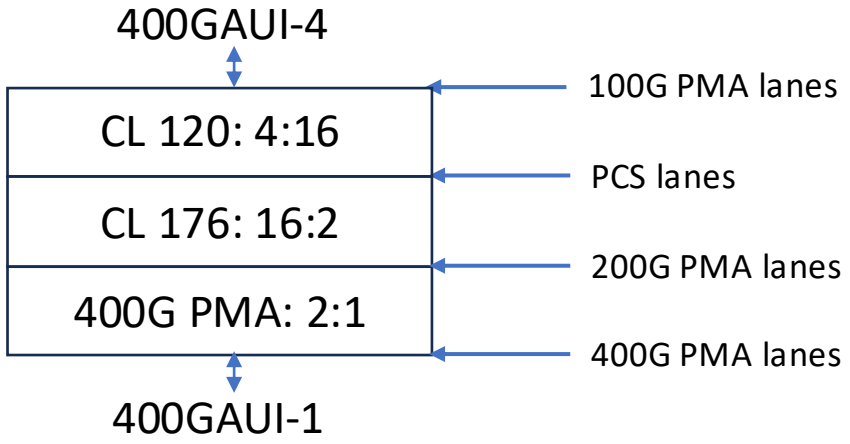




B: 200G PMA to 400G PMA lanes

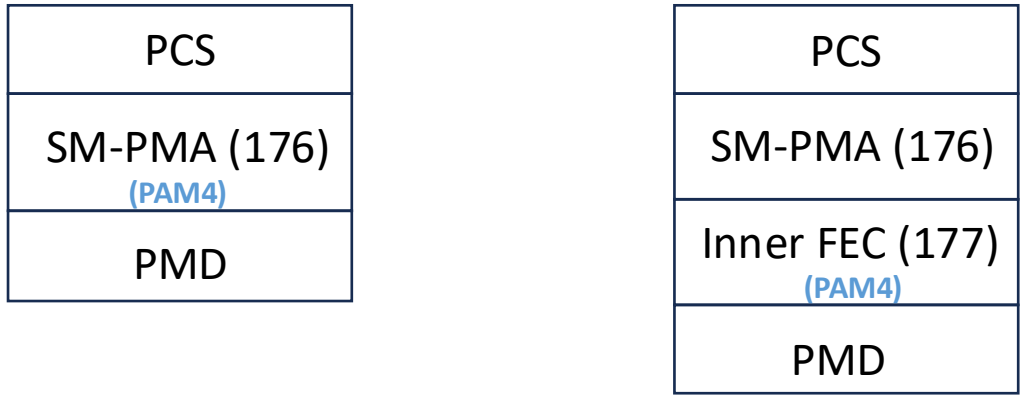
- Single or Multiple PMAs (400GbE)





Handling PAM4 and PAM6 encoding

- What's in 802.3dj : only PAM4
  - PAM4 encoding included in SM-PMA (CL 176)
  - PAM4 encoding also in CL 177 Inner FEC
    - In this case, PMA generates a stream of bits towards Inner FEC (without PAM4 encoding)
  - PAM4 encoding is used for all PMDs



- 802.3dv Logic Architecture should support both PAM4 and PAM6 encoding

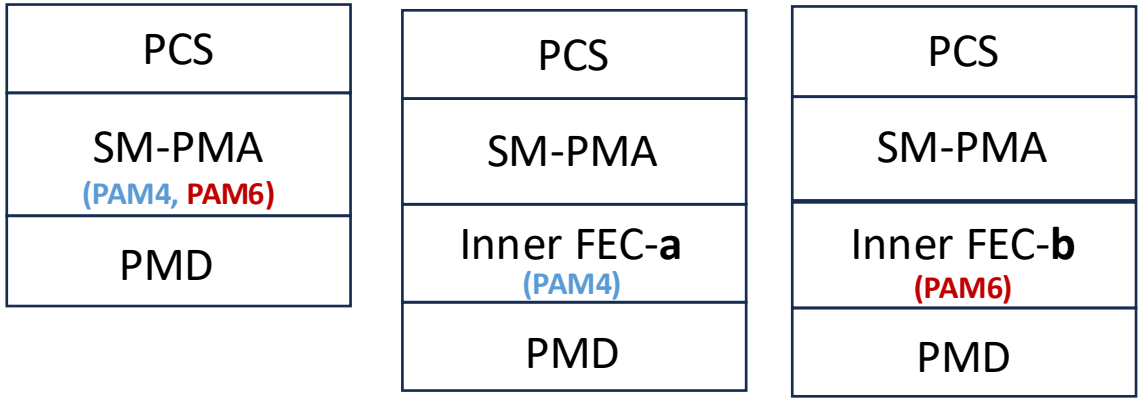
Options to handle PAM4 and PAM6 encoding in 802.3dv

- **Option 1**: Include both PAM4 and PAM6 coding options at 400Gb/s interfaces in the PMA and Inner FEC
  - Following 802.3dj precedent

- **Option 2**: Move PAM4 and PAM6 coding options to separate sublayer (C-PMA)
  - 400G SM-PMA : becomes purely muxing logic
  - New C-PMA : PAM4 or PAM6 coding (including test patterns, loopbacks, etc.)

Option 1: PAM4 and PAM6 encoding in PMA and FECi

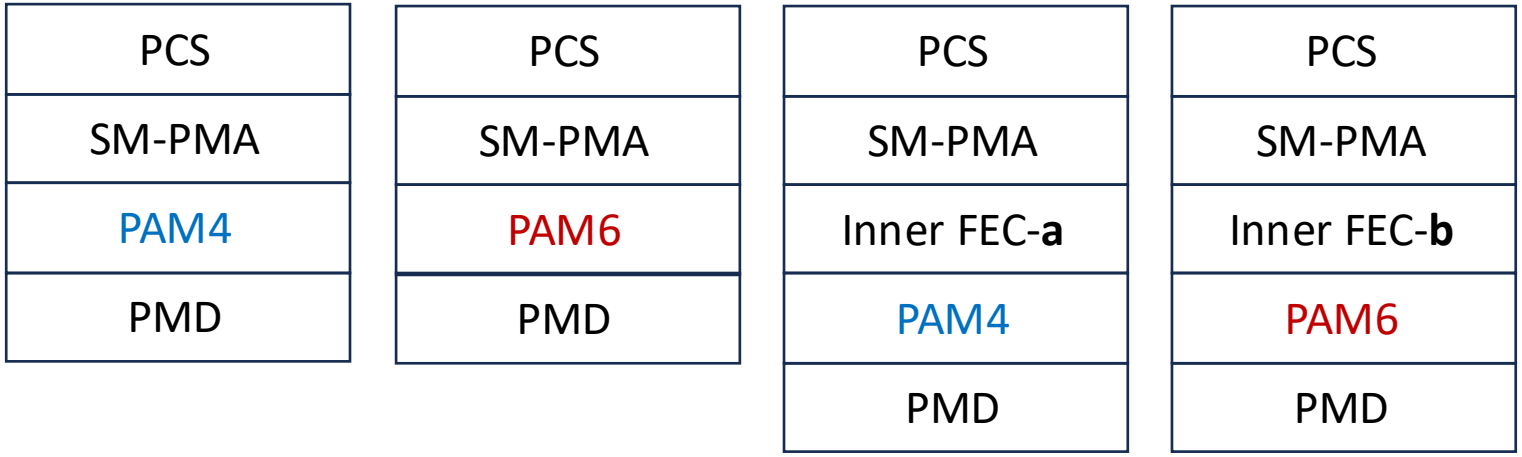
- Keep PAM4/PAM6 in the PMA and Inner FEC – same as 802.3dj



- PAM4/PAM6 encoding in PMA - like in CL 176
  - For PMDs not requiring an Inner FEC
- PAM4/PAM6 in Inner-FEC as needed
  - E.g. Optical PMD or Electrical AUI/PMD with Inner FEC

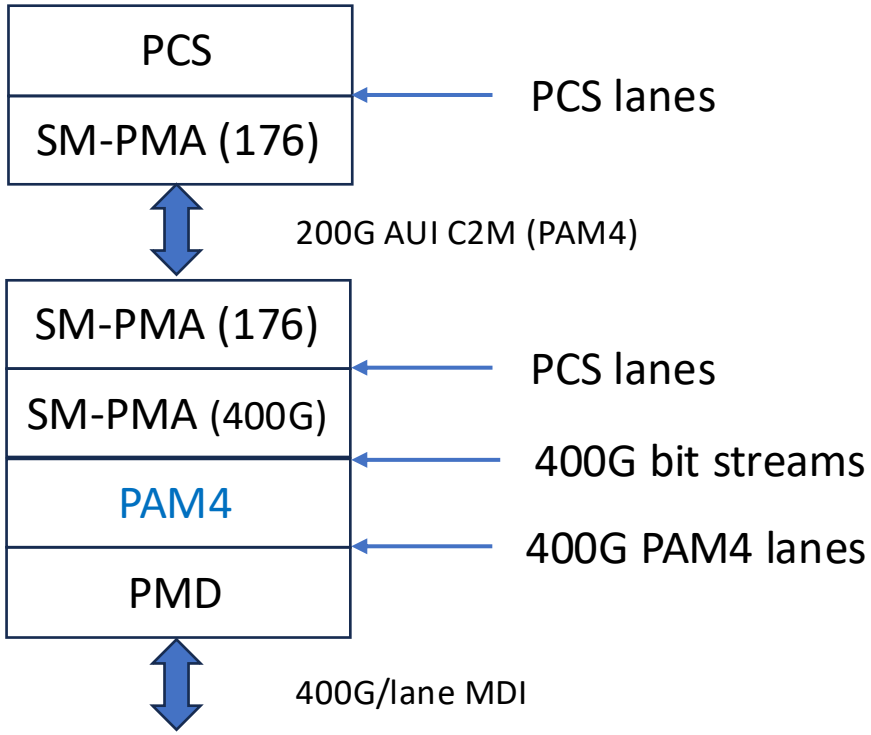
Option 2: PAM4 and PAM6 encoding in separate sublayer

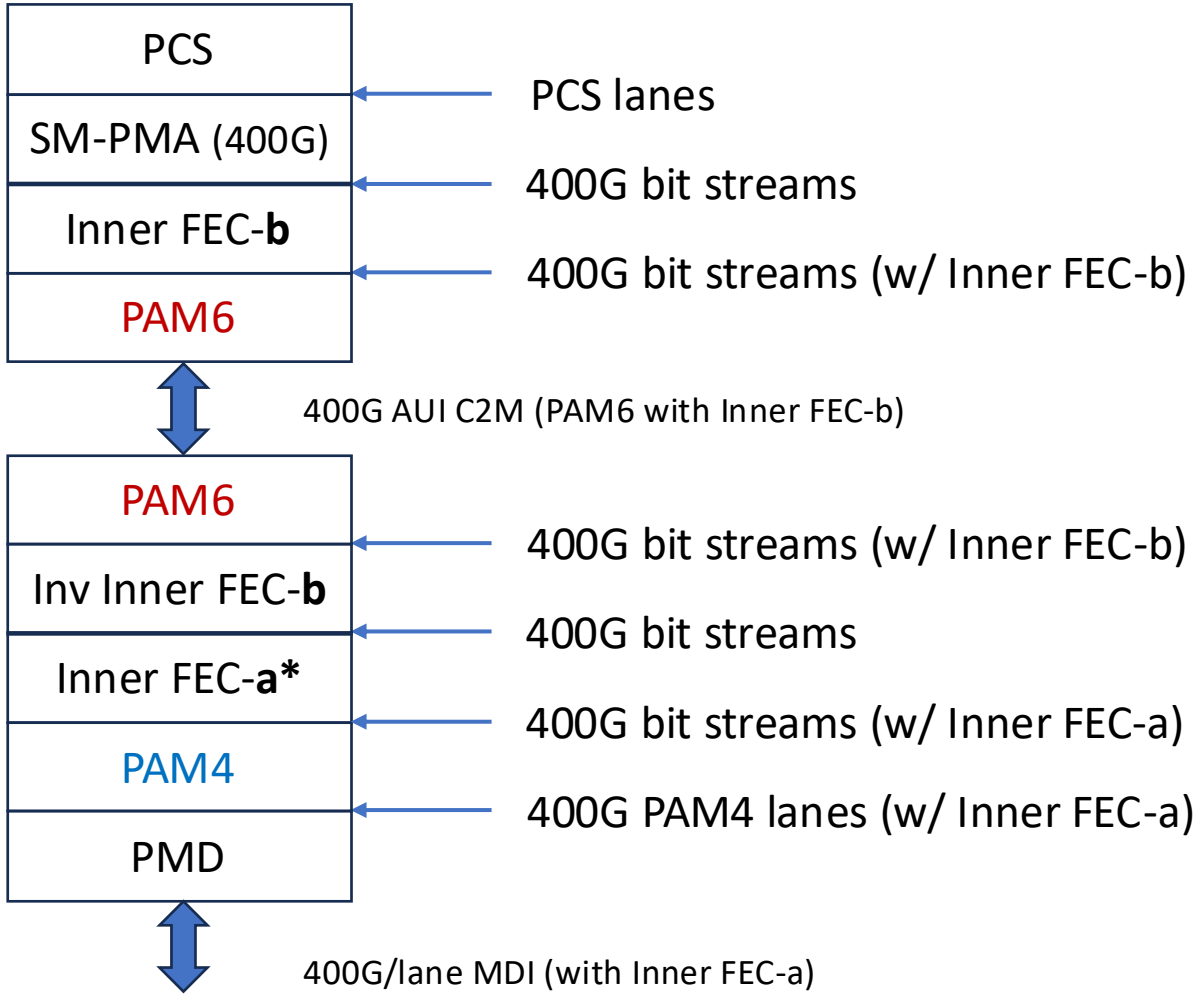
- Move PAM4 and PAM6 coding options to separate sublayer (not in SM-PMA)
  - *Nomenclature TBD – two types of "C-PMA", one for PAM4, one for PAM6*



- SM-PMA has muxing logic only
- PAM-x encode in separate sublayer
- Architecturally clean – can use PAM4 or PAM6 where needed
- Can still use option of combining PAM6 coding with Inner FEC in single sublayer when tightly coupled.

Possible Examples of 400G/lane Stack-ups (Options A & 2)





*Can be Inner FEC or Segmented FEC conditional on PMD type

Summary

- Use 802.3dj Logic Architecture as the starting point
  - Four-codeword Interleaving
  - Symbol-multiplexing of PCS lanes to PMA lanes

- For 802.3dv PMA
  - Should continue to use four-codeword interleaving and symbol multiplexing
  - Options are available for converting PCS lanes to 400G PMA lanes
  - Options are available to support PAM4 and PAM6 coding and Inner FEC(s)
  - Options shown affect the specification description; do not change functionality
  - Logic layering can use these options to adapt to the FEC and modulation that is adopted for the AUIs and PMDs

Thank You