Table 45–20—10P SCM indicator bits status register bit definition

Bit(s)	Name	Description	R/W[a]
1.x.5	IB-8 *(flos_cr2)*	0 = normal state 1 = link partner is reporting loss of carrier 2	RO
1.x.4	IB-9 *(rdi)*	0 = normal state 1 = link partner is reporting the reception of a severely errored PMA frame	RO
1.x.3	IB-10 *(reserved*)	0 = normal state 1 = reserved condition	RO
1.x.2	IB-11 *(reserved*)	0 = normal state 1 = reserved condition	RO
1.x.1	reserved	value always 0	RO
1.x+1.15	reserved	value always 0	RO
1.x+1.14	IB-12 *(FPO)*	0 = normal state 1 = link partner is reporting a Power-off failure	RO
1.x+1.13	IB-13 *(flpr)*	0 = normal state 1 = link partner is reporting a Loss-of-Power defect (dying gasp)	RO
1.x+1.12:9	proprietary	reserved for proprietary application 0 = normal state 1 = unspecified condition	RO
1.x+1.8:0	reserved	value always 0	RO

[a]RO = Read Only

45.2.1.29 10P MCM registers overview

Editor's Note: The value 4098 below was changed in this draft to 2048 reflecting the resolution of comments that set the number of tones for 10PASS-TS MCM to 2048

10P MCM operates by modulating 2048 individual tones across the transmission spectrum. Each tone can be assigned a PSD level, desired SNR margin and transmission direction (downstream or upstream). To reduce the complexity of addressing individual tones, tones are addressed by group. The STA sets the lower and upper tones in a group, sets the parameters for that group, and issues a command to activate those parameters for that group. See Clause 62 (MCM) for details on the mechanism that transfers tone information across the link to and from the "-R" link partner.

Additionally, there is defined a new MMD at address 6, the 10P MCM tone table. The 10P MCM tone table is used to query the status of every tone in the PMD.

45.2.1.30 10P MCM PMA/PMD general configuration register

The 10P MCM PMA/PMD general configuration register is defined only for "-O" port types.

The 10P MCM PMA/PMD general configuration register bit definitions may be found in Table 45–21.

Table 45–21—10P MCM PMA/PMD general configuration register bit definitions

Bit(s)	Name	Description	R/W[a]
1.x.15:8	TX window length	Transmit window length within cyclic prefix and suffix	O: R/W R: undefined
1.x.7:3	reserved	value always 0, writes ignored	R/W
1.x.2:1	FFT/IFFT size	The number of tones of FFT/IFFT: 00 = invalid 01 = 1024 tones 10 = 2048 tones 11 = invalid	O: R/W R: undefined
1.x.0	Tone spacing	0 = 4.3125 KHz (default) 1 = 8.625 KHz	O: R/W R: undefined

[a]R/W = Read/Write

45.2.1.30.1 TX window length (1.x.15:7)

Bits 15:7 control the PMD transmit window length within the cyclic prefix and suffix in units of number of samples, as defined in 62.4.1

45.2.1.30.2 FFT/IFFT size (1.x.2:1)

Bits 2:1 control the PMD FFT/IFFT size as defined in 62.4.4.2.2.

45.2.1.30.3 Tone spacing (1.x.0)

Bit 0 selects the tone spacing to be used by the PMD FFT/IFFT.

45.2.1.31 10P MCM PSD configuration register

The 10P MCM PSD configuration register bit definitions may be found in Table 45–22.

Table 45–22—10P MCM PSD configuration register bit definitions

Bit(s)	Name	Description	R/W[a]
1.x.15:9	reserved	value always 0, writes ignored	R/W
1.x.8	PBO mask select	0 = PBO uses max RX PSD 1 = PBO uses TX PSD	O: R/W R: undefined
1.x.7:0	reserved	value always 0x00, writes ignored	R/W

[a]R/W = Read/Write

45.2.1.31.1 PBO mask select (1.x.8)

Selects the UPBO mode: UPBO based on a maximal allowed upstream transmit PSD or UPBO based on a reference PSD.

45.2.1.32 10P MCM downstream data rate configuration register

The bit definitions for the 10P MCM downstream data rate configuration register are found in Table 45–23.

Table 45–23—10P MCM downstream data rate configuration register bit definitions

Bit(s)	Name	Description	R/W[a]
1.x.15:0	Minimum Downstream Data Rate	sets the required downstream payload data rate M := value of bits Data rate = M x 64000 b/s	O: R/W R: undefined
1.x+1.15:0	Maximum Down-stream Data Rate	sets the maximum downstream payload data rate M := value of bits Data rate = M x 64000 b/s	O: R/W R: undefined

[a]R/W = Read/Write

45.2.1.33 10P MCM downstream RS/interleaver configuration register

The bit definitions for the 10P MCM downstream RS/interleaver configuration register are found in Table 45–24.

Table 45–24—10P MCM downstream RS/interleaver configuration register bit definitions

Bit(s)	Name	Description	R/W[a]
1.x.15:8	RS overhead	overhead = 16, coded as 0x10 all other values: reserved	O: R/W R: undefined
1.x.7:0	RS codeword length	codeword length = 144, coded as 0x90 codeword length = 240, coded as 0xF0 all other values: reserved	O: R/W R: undefined
1.x.15:8	Interleaver parameter *M*	*M* is the value of the bits *M* shall be between 2 and 52 if RS codeword length = 144 *M* shall be between 2 and 62 if RS codeword length = 240 values greater than 62 are reserved	O: R/W R: undefined
1.x.7:0	Interleaver parameter *I*	*I* = 36, coded as 0x24 (mandatory if RS codeword length = 144) *I* = 30; coded as 0x1E (mandatory if RS codeword length = 240) all other values: reserved	O: R/W R: undefined

[a]R/W = Read/Write

45.2.1.34 10P MCM downstream EOC/VOC configuration register

This register is defined only for "-O" ports.

The bit definitions for the 10P MCM downstream EOC/VOC configuration register are found in Table 45–25.

Table 45–25—10P MCM downstream EOC/VOC configuration register

Bit(s)	Name	Description	R/W[a]
1.x.15:9	Max DS EOC frame size	EOC bytes per frame in the downstream direction [T1424, 11.2.6.2.1.1]	O: RW R: undefined
1.x.8:0	Max DS VOC frame size	VOC bytes per frame in the downstream direction [T1424, 11.2.6.2.1.1]	O: RW R: undefined

[a]R/W = Read/Write

45.2.1.34.1 Max DS EOC frame size (1.x.15:9)

Bits 15:9 set the maximum size of the EOC portion in the downstream PMA frame. See 62.2.4.5.

45.2.1.34.2 Max DS VOC frame size (1.x.8:0)

Bits 8:0 set the maximum size of the VOC portion in the downstream PMA frame. See 62.2.4.5.

45.2.1.35 10P MCM upstream data rate configuration register

The bit definitions for the 10P MCM upstream data rate configuration register are found in Table 45–26.

Table 45–26—10P MCM upstream data rate configuration register bit definitions

Bit(s)	Name	Description	R/W[a]
1.x.15:0	Minimum Upstream Data Rate	sets the required upstream payload data rate M := value of bits Data rate = M x 64000 b/s	O: R/W R: undefined
1.x+1.15:0	Maximum Upstream Data Rate	sets the maximum upstream payload data rate M := value of bits Data rate = M x 64000 b/s	O: R/W R: undefined

[a]R/W = Read/Write

45.2.1.36 10P MCM upstream RS/interleaver configuration register

The bit definitions for the 10P MCM upstream RS/interleaver configuration register are found in Table 45–27.

45.2.1.37 10P MCM upstream EOC/VOC configuration register

This register is defined only for "-O" ports.

The bit definitions for the 10P MCM upstream EOC/VOC configuration register are found in Table 45–28.

Table 45–27—10P MCM upstream RS/interleaver configuration register bit definitions

Bit(s)	Name	Description	R/W[a]
1.x.15:8	RS overhead	overhead = 16, coded as 0x10 all other values: reserved	O: R/W R: undefined
1.x.7:0	RS codeword length	codeword length = 144, coded as 0x90 codeword length = 240, coded as 0xF0 all other values: reserved	O: R/W R: undefined
1.x.15:8	Interleaver parameter *M*	*M* is the value of the bits *M* shall be between 2 and 52 if RS codeword length = 144 *M* shall be between 2 and 62 if RS codeword length = 240 values greater than 62 are reserved	O: R/W R: undefined
1.x.7:0	Interleaver parameter *I*	*I* = 36, coded as 0x24 (mandatory if RS codeword length = 144) *I* = 30; coded as 0x1E (mandatory if RS codeword length = 240) all other values: reserved	O: R/W R: undefined

[a]R/W = Read/Write

Table 45–28—10P MCM upstream EOC/VOC configuration register

Bit(s)	Name	Description	R/W[a]
1.x.15:9	Max US EOC frame size	EOC bytes per frame in the upstream direction [T1424, 11.2.6.2.1.1]	O: R/W R: undefined
1.x.8:0	Max US VOC frame size	VOC bytes per frame in the upstream direction [T1424, 11.2.6.2.1.1]	O: R/W R: undefined

[a]R/W = Read/Write

45.2.1.37.1 Max US EOC frame size (1.x.15:9)

Bits 15:9 set the maximum size of the EOC portion in the upstream PMA frame. See 62.2.4.5.

45.2.1.37.2 Max US VOC frame size (1.x.8:0)

Bits 8:0 set the maximum size of the VOC portion in the upstream PMA frame. See 62.2.4.5.

45.2.1.38 10P MCM tone group register

This register allows the STA to specify the range of tones to control. The bit definitions for the 10P MCM tone group register are defined in Table 45–29.

This register is defined only for "-O" ports.

45.2.1.39 10P MCM tone control parameter register

This register allows the STA to specify values for various parameters for the tones selected in the 10P MCM tone group register. These values do not take effect until the corresponding activation commands are issued in the 10P MCM tone control action register. The bit definitions for the 10P MCM tone control parameter register are shown in Table 45–30.

Table 45–29—10P MCM tone group register bit definitions

Bit(s)	Name	Description	R/W[a]
1.x.15:0	Lower tone	The number of the lower frequency tone in the group. Valid when <= the Upper tone.	R/W
1.x+1.15:0	Upper tone	The number of the higher frequency tone in the group. Valid when >= the Lower tone.	R/W

[a]R/W = Read/Write

This register is defined for only "-O" ports.

Table 45–30—10P MCM tone control parameter register bit definitions

Bit(s)	Name	Description	R/W[a]
1.x.15	Tone active	0 = selected tones are disabled 1 = selected tones are active	R/W
1.x.14	Tone direction	0 = selected tones are assigned for DS communication 1 = selected tones are assigned for US communication	R/W
1.x.13:5	Max SNR margin	Assigns the maximum SNR margin the tones shall achieve M := value of bits Max SNR Margin = M/4 dB	R/W
1.x.4:0, 1.x+1.15:12	Target SNR margin	Assigns the target SNR margin for the selected tones M := value of bits Min SNR Margin = M/4 dB	R/W
1.x.4:0, 1.x+1.11:3	Min SNR margin	Assigns the minimum SNR margin for the selected tones M := value of bits Min SNR Margin = M/4 dB	R/W
1.x+1.2	reserved	value always 0, writes ignored	R/W
2.x+1.1:0 1.x+2.15:9	PSD level	Assigns a TX PSD level for the selected tones in dBm/Hz P := value of bits (2's complement) PSD Level = P/4 - 100 dBm/Hz	R/W
1.x+2.8:0	UPBO reference	Assigns the level of the UPBO reference at the points represented by the selected tones P := value of bits (2's complement) PSD Level = P/4 - 100 dBm/Hz	R/W

[a]R/W = Read/Write

45.2.1.40 10P MCM tone control action register

The bit definitions for the 10P MCM tone control action register are shown in Table 45–31.

This register is defined for only "-O" ports.

Table 45–31—10P MCM tone control action register bit definitions

Bit(s)	Name	Description	R/W[a]
1.x.15:6	reserved	Value always 0, writes ignored	R/W
1.x.5	Refresh tone table	1 = refresh the contents of the selected tones' entries in the Tone Table 0 = ready, operation complete Note: Refreshing a large number of tones may take a long time to complete.	R/W, SC
1.x.4	Change tone activity	1 = activate Tone active setting as in Tone Control Parameter reg. 0 = ready, operation complete	R/W, SC
1.x.3	Change tone direction	1 = activate Tone direction setting as in Tone Control Parameter reg. 0 = ready, operation complete	R/W, SC
1.x.2	Change SNR margin	1 = activate Min, Max and Target SNR margin settings as in Tone Control Parameter register 0 = ready, operation complete	R/W, SC
1.x.1	Change PSD level	1 = activate PSD level setting as in Tone Control Parameter reg. 0 = ready, operation complete	R/W, SC
1.x.0	Change UPBO Reference PSD	1 = activate UPBO Reference PSD settings as in Tone Control Parameter reg. 0 = ready, operation complete	R/W, SC

[a]R/W = Read/Write, SC = Self Clearing

45.2.1.41 10P MCM indicator bits status register

The 10P MCM indicator bits status register conveys the current state of the indicator bits being sent over the link by the local PMA and received on the link from the remote PMA. (See 62.2.4) The bit definitions for the 10P MCM indicator bits status register are shown in Table 45–32.

Table 45–32—10P MCM indicator bits status register bit definition

Bit(s)	Name	Description	R/W[a]
1.x.15-9	reserved	Reserved for future use.	RO
1.x.8	LoM	0 = normal state 1 = link partner is reporting loss of margin	RO
1.x.7	Flpr	0 = normal state 1 = link partner is reporting that the 10PASS-TS power supply (mains) voltage drops below the manufacture-determined level required for proper PHY operation.	RO
1.x.6	Fpo	0 = normal state 1 = link partner is reporting that the power switch was turned off at the far end	RO
1.x.5	Rdi	0 = normal state 1 = link partner is reporting severe frame errors at the far end	RO
1.x.4	Flos	0 = normal state 1 = link partner is reporting that the received 10PASS-TS signal power is lower than the threshold	RO
1.x.3	Ffec-f	0 = normal state 1 = reserved condition	RO
1.x.2	Febe-f	0 = normal state 1 = reserved condition	RO
1.x.1	Ffec-s	0 = normal state 1 = link partner is reporting that errored octets corrected by FEC have been detected in the received block of slow data	RO
1.x.0	Febe-s	0 = normal state 1 = link partner is reporting that non-corrected errors have been detected in the received block of slow data	RO

[a]RO = Read Only

45.2.1.42 2B general parameter register

The 2B general parameter register controls various parameters for the operation of the 2BASE-TL PMA/PMD. **See (REFERENCE REQUiRED)**

This register is read only for "-R" ports which may be read so the STA may know the mode selected by the "-O" port. The selected parameters on the "-O" are sent to the "-R" link partner on link initialization.

The bit definitions for the 2B general parameter register are found in Table 45–49.

Ed Note: The "Profile select" bits were removed from the 2B general parameter register for D1.732. Profiles are programmed using the parameter registers.

45.2.1.43 2B PMD parameters register

The 2B PMD parameters register sets the transmission parameters for the PMD. When the link is initialized or reset, these parameters shall be used by the PHY transmitter. Since writing to this register does not have an immediate effect, reading this register returns the desired parameters, which are not necessarily the current operating parameters.