PAF_BadFragmentReceived: this signal is asserted to indicate that a fragment has been received which does not fit into the sequence expected by the frame assembly function. The errored fragment has been discarded and the frame buffer flushed to the next valid frame start. The corresponding register is defined in ~~45.2.3.28~~45.2.3.28.

PAF_LostFragment: this signal is asserted to indicate that a fragment (or fragments) expected according to sequence has not been received by the frame assembly function. The missing fragment (or fragments) has been skipped and the frame buffer flushed to the next valid frame start. The corresponding register is defined in ~~45.2.3.29~~45.2.3.29.

PAF_LostStart: this signal is asserted to indicate that the packet reassembly function did not receive a StartOf Packet indicator in the appropriate sequence. The corresponding register is defined in ~~45.2.3.30~~45.2.3.30.

PAF_LostEnd: this signal is asserted to indicate that the packet reassembly function did not receive an End-OfPacket indicator in the appropriate sequence. The corresponding register is defined in ~~45.2.3.31~~45.2.3.31.

61.2.2.7.3 PHY PMI aggregation register functions

~~Clause 45~~Clause 45 defines two bits in the EFM copper control register (see ~~45.2.3.18~~45.2.3.18) to control the PAF function. PAF_available is used to indicate that the system has the capability to aggregate PMIs, PAF_enable is used to control whether this ability is enabled or not. In all cases, the PAF_available bit is read-only; the PAF_enable bit is read-only unless the PAF_available bit is asserted, in which case the PAF_enable bit is write/read.

For CO-subtype devices, both the PAF_available and the PAF_enable bits are only accessible locally, the PAF_enable bit is writeable.

For CPE-subtype devices, both the PAF_available and the PAF_enable bits are locally read only and remotely readable. The PAF_enable bit is remotely writeable.

~~Clause 45~~Clause 45 defines 2 registers which relate to the PHY PMI aggregation function: the PMI_Available_register (see ~~45.2.3.20~~45.2.3.20) and the PMI_Aggregate_register (see ~~45.2.3.21~~45.2.3.21). Additionally the remote_discovery_register and Aggregation_link_state_register shall be implemented.

The PMI_Available_register is read-only for CO-subtype and may be writeable for CPE-subtype (in order to restrict CPE-subtype connection capability according to ~~45.2.3.20~~45.2.3.20). It indicates whether an aggregateable link is possible between this PCS and multiple PMD's. For a device that does not support aggregation of multiple PMIs, a single bit of this register shall be set and all other bits clear. The position of bits indicating aggregateable PMI links correspond to the PMA/PMD sub-address defined in ~~Clause 45~~Clause 45.

For CPE-subtype devices, the PMI_Available_register may optionally be writeable by the local management entity. The reset state of the register reflects the capabilities of the device. The management entity (through ~~Clause 45~~Clause 45 access) may clear bits which are set, in order to limit the mapping between MII and PMI for PMI aggregation. For CPE-subtype devices, PMD links shall not be enabled (such that no handshaking starts) until the PMI_Available register has been set to limit the connectivity such that each PMI maps to one, and only one MII (~~45.2.3.20~~45.2.3.20).For CPE-subtype devices, until this conditions is met, the deivce shall not repond to or initiate any G.994.1 handshaking sessions, on any of its PMI's. Multiple PMI's per MII are allowed.

The PMI_Aggregate_register is defined in ~~Clause 45~~Clause 45. For CO-subtype devices, access to this register is through ~~Clause 45~~Clause 45 register read and write mechanisms. For CPE-subtype devices the register may be read locally through ~~Clause 45~~Clause 45, reads and writes shall be allowed from remote devices

via the remote access signals passed across the γ-interface from the PMA (see 61.2.3.1). The operation of the PMI_Aggregate_register for CPE-subtype devices is defined as follows:

a) If the remote_discovery_register is clear then the PMI_Aggregate_register shall be cleared.

b) If write_remote_Aggregation_reg is asserted, the contents of remote_write_data bit zero is written to ~~PMI_Aggregation_register~~ PMI_Aggregate_register in the bit location corresponding to the PMA/PMD from which the request was received. Acknowledge_read_write is asserted for one octet clock cycle.

c) If read_remote_Aggregation_reg is asserted, the contents of ~~PMI_Aggregation_register~~ PMI_Aggregate_register are placed onto remote_read_data bus, bits 31 through 0. Unsupported bits are written as zero if the full width of PMI_Aggregation_register is not supported. Acknowledge_read_write is asserted for one octet clock cycle.

The remote_discovery_register shall be implemented for CPE-subtype devices. The remote_discovery_register may be read locally through ~~Clause 45~~Clause 45 register access mechanisms. The remote_discovery_register shall support atomic write operations and reads from remote devices via the remote access signals passed across the γ-interface from the PMA (see 61.2.3.1). The operation of the remote_discovery_register for CPE-subtype devices is defined as follows:

a) If read_remote_discovery_reg is asserted, the contents of remote_discovery_register are placed onto remote_read_data bus. Acknowledge_read_write is asserted for one octet clock cycle.

b) If write_remote_discovery_reg is asserted, the action depends on the contents of remote_discovery_register. If the remote_discovery_register is currently clear (no bits asserted), the contents of the remote_write_data bus are placed into the remote_discovery_register. The new contents of remote_discovery_register are placed on the remote_read_data bus. Acknowledge_read_write is asserted for one octet clock cycle. Else if the remote_discovery_register is not currently clear (any bit asserted), no data is written. The old contents of remote_discovery_register are placed on the remote_read_data bus. NAcknowledge_read_write is asserted for one octet clock cycle. If multiple write_remote_discovery_reg signals are asserted (from multiple γ-interfaces) they shall be acted upon serially.

~~c) If clear_remote_discovery_reg is asserted, the remote_discovery_register is cleared. The new contents of remote_discovery_register are placed on the remote_read_data bus. Acknowledge_read_write is asserted for one octet clock cycle.~~

d) If clear_remote_discovery_reg is asserted, the action depends on the contents of remote_discovery_register. If the contents of the remote_write_data bus match that of the the remote_discovery_register, the remote_discovery_register is cleared, the PMI_Aggregate_register is cleared, the new contents of remote_discovery_register are placed on the remote_read_data bus, and Acknowledge_read_write is asserted for one octet clock cycle. If the contents of the remote_write_data bus do not match that of the the remote_discovery_register, the remote_discovery_register is unchanged, its contents are placed on the remote_read_data bus, and NAcknowledge_read_write is asserted for one octet clock cycle.

e) If the logical AND of the Aggregation_link_state_register and the PMI_Aggregate_register is clear then a timeout counter shall be started. If this condition continues for 30 seconds (the timeout period) then the remote_discovery_register shall be cleared.

Note that a single device may be implemented which has multiple MII interfaces and (therefore) multiple PCS instances. There shall be one remote_disovery_register per PCS instance. The PMI_Available_register shall be set prior to the enabling of links so that each PMA/PMD is linked to only one PCS. Access to the remote_discovery_register (read or write) shall be restricted to PMA/PMD instances for which the corresponding PMI_Available_register bit is asserted.

The Aggregation_link_state_register is a pseudo-register corresponding to the PCS_link_state bits from each γ-interface in the appropriate bit positions according to the PMA/PMD from which the signal is received. Bits corresponding to unsupported aggregation connections are zero.

The remote access mechanisms for the PMI aggregation registers are defined in 61.3.12.