Insert the following new registers, descriptions and tables after 45.2.1.10:

45.2.1.11 10P/2B PMA/PMD status register

The assignment of bits in the 10P/2B PMA status register is shown in Table 45–3.

Table 45–3—10P/2B PMA status register bit definitions

Bit(s)	Name	Description	R/W[a]
1.x.15	10PASS-TS supported	0 = PHY incapable of 10PASS-TS 1 = PHY capable of 10PASS-TS	RO
1.x.14	2BASE-TL supported	0 = PHY incapable of 2BASE-TL 1 = PHY capable of 2BASE-TL	RO
1.x.13:2	reserved	Value always 0, writes ignored	R/W
1.x.1:0	PMA/PMD link status	0 = link is ~~down or initializing~~Down 1 = link is ~~up~~Initializing 2 = link is Up, 10PASS-TS 3 = link is Up, 2BASE-TL	RO
~~1.x.0~~	~~Handshake result~~	~~0 = handshake unsuccessful~~ ~~1 = handshake completed successfully~~	~~RO, LH~~

[a]RO = Read Only, LH = Latches High

45.2.1.11.1 10PASS-TS supported (1.x.15)

A one in bit 15 indicates that the PHY supports the 10PASS-TS PMA/PMD as defined in *CROSS REF Clause 62*.

45.2.1.11.2 2BASE-TL supported (1.x.14)

A one in bit 15 indicates that the PHY supports the 2BASE-TL PMA/PMD as defined in *CROSS REF Clause 63*.

45.2.1.11.3 PMA/PMD link status (1.x.1)

The overall state of the PMA/PMD link is reflected in bit 11. After the PMA/PMD is operationally linked to the remote PHY, the PHY shall set this bit to a one. In all other cases, this bit shall remain zero.

45.2.1.11.4 Handshake result (1.x.0)

The STA may read the result of the handshake operation in bit 9. Upon reset or an unsuccessful handshake, the PHY shall set this bit to zero. Upon completion of a successful handshake, the PHY shall set this bit to a one.

45.2.1.12 10P/2B PMA/PMD control register

The assignment of bits in the 10P/2B PMA control register is shown in Table 45–4.

Table 45–4—10P/2B PMA control register bit definitions

Bit(s)	Name	Description	R/W[a]
1.x.15:13	PMA/PMD type selection	15 14 13 0 0 0 = 10PASS-TS PMA/PMD type 0 0 1 = 2BASE-TL PMA/PMD type 0 1 0 = 2BASE-TL or 10PASS-TS (NT only) 0 1 1 = 2BASE-TL preferred,or 10PASS-TS (LT only) 1 0 0 = 10PASS-TS preferred, or 2BASE-TL (LT only) all other values are reserved	R/W
1.x.12	PMA/PMD link control	0 = force link down 1 = initiate link	R/W
1.x.11	reserved	Value always 0, writes ignored	R/W
~~1.x.10~~	~~Handshake control~~	~~0 = stop handshake or handshake inactive~~ ~~1 = start handshake or handshake in progress~~	~~R/W, SC~~
1.x.~~9~~10:0	reserved	Value always 0, writes ignored	R/W

[a]R/W = Read/Write, SC = Self Clearing

45.2.1.12.1 PMA/PMD type selection (1.x.15:13)

The PMA/PMD type of a 10P/2B PHY may be selected using bits 15 through 13. A PHY may ignore writes to the type selection bits that select PMA/PMD types it has not advertised in the status register. It is the responsibility of the STA entity to ensure that mutually acceptable MMD types are applied consistently across all the MMDs on a particular PHY.

The selection is advertised during link initialization G.994 handshake.

The PMA/PMD type selection defaults to a supported ability.

45.2.1.12.2 PMA/PMD link control (1.x.12)

The mode of the PMA/PMD link is controlled by setting bit 12. The PHY shall ignore a write to this bit if handshake is in progress (bit 10).

45.2.1.12.3 Handshake control(1.x.10)

If PMA/PMD link is forced down by bit 12, then bit 10 may be used to initiate handshake as in *CROSS REF* 61.3. While handshake is in progress this bit remains set as one. When the modem is reset or after handshake has completed, the PHY shall set this bit back to zero. Clearing this bit to a zero while it is set to one (handshake in progress) shall cause G.994.1 cleardown, terminating the handshake.

45.2.1.13 10P/2B PMA/PMD link loss register

The 10P/2B PMA/PMD link loss register is a 16 bit counter that contains the number of times the PMA/PMD has lost link. Link shall be considered lost when the PMA_receive_synchronized signal is false (*CROSS REF 61.2.3.2.1)* These bits shall be reset to all zeroes when the register is read by the management function or upon execution of the MMD reset. These bits shall be held at all ones in the case of overflow. The assignment of bits in the 10P/2B PMA/PMD link loss register is shown in Table 45–5.

45.2.3.17 Coding violation counter register. (3.x)

Table 45–202—Coding violation counter register bit definitions

Bit(s)	Name	Description	R/W[a]
3.x.15:0	Coding violation counter	Error counter	RO, NR

[a]RO = Read Only, , NR = Non Roll-over

The assignment of bits in the coding violation counter register is shown in Table 45–202. The coding violation counter is a sixteen bit counter that contains the number of coding violations received during normal operation (see 24.2.2.1.7 or 36.2.4.19). These bits shall be reset to all zeroes when the coding violation counter is read by the management function or upon execution of the PCS reset. These bits shall be held at all ones in the case of overflow.

45.2.3.18 10P/2B capability register (3.x)

The 10P/2B capability register controls general functions of the PHY. This register is present at the PCS layer for each PHY. The bit definitions of the 10P/2B capability register are shown in Table 45–203.

Table 45–203—10P/2B capability register bit definitions

Bit(s)	Name	Description	R/W[a]
3.x.15	Port sub-type select	0 = port shall operate as a R sub-type 1 = port shall operate as an O sub-type	R/W
3.x.14	CO supported	0 = CO subtype operation not supported 1 = CO subtype operation supported	RO
3.x.13	CPE supported	0 = CPE subtype operation not supported 1 = CPE subtype operation supported	RO
3.x.12	PAF supported	0 = PAF not supported 1 = PAF supported	RO
3.x.11	Remote PAF supported	0 = link partner does no support PAF 1 = link partner supports PAF	RO
3.x.10	PAF enable	0 = do not use PAF 1 = use PAF	O: R/W R: R/O
3.x.9:0	reserved	Value always 0, writes ignored	R/W

[a]R/W = Read/Write, RO = Read Only

45.2.3.18.1 Port sub-type select (3.x.15)

This register bit selects the port sub-type for PHY operation. See *CROSS REF* ~~61.1~~61.1 for more information on 10PASS-TS/2BASE-TL port sub-types. The bit defaults to a supported mode. The PHY shall ignore writes that select an unsupported mode.

45.2.3.18.2 CO supported (3.x.14)

This bit indicates that the PHY supports operation as a CO subtype. The PHY sets this bit to a one when the capability is supported and zero otherwise. See *CROSS REF* 61.1.5.5.

45.2.3.18.3 CPE supported (3.x.13)

This bit indicates that the PHY supports operation as a CPE subtype. The PHY sets this bit to a one when the capability is supported and zero otherwise. See *CROSS REF* 61.1.5.5.

45.2.3.18.4 PAF supported (3.x.12)

This bit indicates that the PHY supports the PMI aggregation function. The PHY sets this bit to a one when the capability is supported and zero otherwise. See *CROSS REF* 61.1.5.4.

45.2.3.18.5 Remote PAF supported (3.x.12)

This bit ~~shall indicate~~ indicates that the remote, link-partner PHY supports the PMI aggregation function. The PHY sets this bit to a one when the capability is supported and zero otherwise. This bit ~~shall~~ does not ~~be set until handshake has completed and discovered~~ accurately report the capability of the remote PCS until remote PMI Aggregation register access has been attempted by the "-O" PHY. In this case, this bit is set in the CPE device if the PAF-O supported bit is set in the capabilities exchange, while this bit is set in the CO device if the PMI Aggregate or Remote Discovery SPar(2) bits are set in the CLR meesages. See *CROSS REF* 61.1.5.4.

45.2.3.18.6 PAF enable (3.x.10)

Setting this bit to a one shall activate the PMI aggregation function of the PCS when the link is established. Writes to this bit while link is active or if the PAF is not supported shall be ignored. When link is established, handshake indicates the use of PAF to the ~~remote~~ "-R" PHY. See *CROSS REF* 61.1.5.4.

45.2.3.19 10P/2B PHY-MAC rate matching register

The assignment of bits in the 10P/2B PHY-MAC rate matching register is shown in Table 45–204.

Table 45–204—10P/2B PHY-MAC rate matching register bit definitions

Bit(s)	Name	Description	R/W[a]
3.44.15	MII receive during transmit	1 = MII can TX/RX simultaneously 0 = MII cannot TX/RX simultaneously. (default)	R/W
3.44.14	TX_EN and CRS infer a collision	1 = MII uses TX_EN and CRS to infer a collision 0 = MII uses COL to indicate a collision (default)	R/W
3.44.13:0	Reserved	Value always 0, writes ignored	R/W

[a]R/W = Read/Write

45.2.3.19.1 MII receive during transmit (3.44.15)

This register bit is used to tell the PHY-MAC rate matching function if the MAC is capable of receiving frames from the PHY while the MAC is transmitting (i.e. sending frames to the PHY). The variable

tx_rx_simultaneously for the PHY-MAC Rate-Matching function takes on the value of this bit as defined in ~~61.2.1.3.2~~61.2.1.3.2

45.2.3.19.2 TX_EN and CRS infer a collision (3.44.14)

This bit is set for exposed MAC-PHY interfaces that do not have a separate collision signal but infer a collision when TX_EN and CRS are asserted simultaneously. The variable crs_and_tx_en_infer_col in the PHY-MAC Rate-Matching function takes on the value of this bit as in ~~61.2.1.3.2~~61.2.1.3.2.

45.2.3.20 10P/2B PMI available register (3.x)

The 10P/2B PMI available register is used to indicate which other PMIs in the aggregation group are available to be aggregated with the queried PMI. A PMI is marked as unavailable if: the PMI does not support PMI aggregation or if the PMI is currently marked to be aggregated with another PMD.

This register may be writable for "-R" ports. For PMIs that may be accessed through more than one MII, the availability is limited such that no PMI may be mapped to more than one MII prior to enabling the links. In this case, the reset state of the 10P/2B PMI available register shall reflect the capabilities of the device, the management entity should reset appropriate bits to meet the restriction described.

If the "-R" device is not capable of aggregating PMIs to multiple MIIs then the 10P/2B PMI available register may be read only.

The 10P/2B PMI available register shall be implemented as a single instance across all PCS MMDs in a package. Reads and writes to any PCS MMD in the same package shall affect this single instance equally. For example, a package implementing four EFM Cu PHYs would have only one 10P/2B PMI available register, addressed by a read or write to 3.45 on any of those PHYs.

The assignment of bits in the 10P/2B PMI Available registers is shown in Table 45–205.

Table 45–205—10P/2B PMI available register bit definitions

Bit(s)	Name	Description	R/W[a]
3.45.15:0	PMI [p = 32:17] available	For each bit in the sequence: 1 = PMI[p] is available for aggregating 0 = PMI[p] is unavailable	O: RO R: R/W
3.46.15:0	PMI [p = 16:1] available	For each bit in the sequence: 1 = PMI[p] is available for aggregating 0 = PMI[p] is unavailable	O: RO R: R/W

[a]RO = Read Only, R/W = Read/Write

45.2.3.21 10P/2B PMI aggregate register

The 10P/2B PMI aggregate register is used to turn on PMI aggregation between the addressed PMI and other PMIs in the aggregation group. Attempts to activate aggregation with an unavailable PMI (See 45.2.3.20) are ignored.

The 10P/2B PMI aggregate register shall be implemented as a single instance across all PCS MMDs in a package. Reads and writes to any PCS MMD in the same package affect this single instance equally. For

example, a package implementing four EFM Cu PHYs would have only one 10P/2B PMI aggregate register, accessed by a read or write to 3.47 on any of those PHYs.

No PMI Aggregate bits need be set if the PAF is disabled.

The assignment of bits for the 10P/2B PMI aggregate register is shown in Table 45–206

Table 45–206—10P/2B PMI aggregate register bit definitions

Bit(s)	Name	Description	R/W[a]
3.47.15:0	Aggregate with PMI [p = 32:17]	For each bit in the sequence: 1 = activate aggregation with PMI[p] 0 = deactivate aggregation with PMI[p]	R/W
3.48.15:0	Aggregate with PMI [p = 16:1]	For each bit in the sequence: 1 = activate aggregation with PMI[p] 0 = deactivate aggregation with PMI[p]	R/W

[a]R/W = Read/Write

45.2.3.22 10P/2B aggregation discovery control register (3.x)

The 10P/2B aggregation discovery control register allows the STA of an "-O" port to determine the aggregation capabilities of an "-R" link-partner.

The 10P/2B aggregation discovery control register shall be implemented as a unique register for each PCS MMDs in a package. For example, a package implementing four EFM Cu PHYs would have four independent instances of the 10P/2B aggregation discovery control register, accessed by a read or write to 3.49 to each PHY.

This register is defined only for "-O" ports. The register bit definitions for the 10P/2B aggregation discovery control register are shown in Table 45–207

Table 45–207—10P/2B aggregation discovery control register bit definitions

Bit(s)	Name	Description	R/W[a]
3.49.15:14	Discovery operation	01 = Ready (default) 00 = Set if clear 11 = Clear if same 10 = Get	R/W
3.49.13	Discovery operation result	0 = discovery operation completed successfully (default) 1 = operation unsuccessful	RO, LH
3.49.12:0	reserved	Value always 0, writes ignored	R/W

[a]R/W = Read/Write, RO = Read Only, LH = Latches High

45.2.3.22.1 Discovery operation (3.x.15:14)

The Discovery operation bits are used to query and manipulate the remote discovery register. The remote discover register is not a Clause 45 object, but a variable of the PMI Aggregation PCS function on "-R"

ports. The "-O" device can perform the query via G.994.1 handshake messages when the link status is down (i.e., neither Initializing nor Up).

The default state of these bits is "Ready." The bits shall indicate "Ready" any time the PMI aggregation function is capable of performing an operation on the remote discovery register.

If the STA sets the bits to "Get," the PMI aggregation function querys the remote discovery register and return its contents to the aggregation discovery code register.

If the STA sets the bits to "Set if clear," the PMI aggregation function passes a message to the "-R" PCS instructing it to set the remote discovery register to the contents of the aggregation discovery code register, but only if the remote discovery register is clear (0x000000000000)

If the STA sets the bits to "Clear if same," the PMI aggregation function passes a message to the "-R" PCS instructing it to clear the remote discovery register, but only if the contents of the remote discovery register currently match the contents of the aggregation discovery code register.

While the requested operation is in progress, the PHY maintains the operation value in the bits. After the operation is complete, the PHY shall set the bits to indicate "Ready"

45.2.3.22.2 Discovery operation result (3.x.13)

When a discovery operation is complete, the PHY sets this bit to indicate the result of the operation. A "1" indicates that the operation could not be completed. This may be for a variety of reasons:

~~a) link is down~~

a) PMA/PMD link status is Initializing or Up

b) a "Set if clear" operation was requested but the remote discovery register was not clear

c) a "Clear if same" operation was requested but the remote discovery register did not match the aggregation discovery code register.

45.2.3.23 10P/2B aggregation discovery code register (3.x)

The 10P/2B aggregation discovery code register stores the code used by the PMI aggregation discovery mechanism.

This register is defined only for "-O" ports.

The 10P/2B aggregation discovery code register shall be implemented as a unique register for each PCS MMDs in a package. For example, a package implementing four EFM Cu PHYs would have four independent instances of the 10P/2B aggregation discovery code register, accessed by a read or write to 3.50 to each PHY

The assignment of bits for the 10P/2B aggregation discovery code register is shown in Table 45–208.

Table 45–208—10P/2B aggregation discovery code register bit definitions

Bit(s)	Name	Description	R/W[a]
3.50.15:0	Code[47:32]	The two most significant octets of the aggregation discovery code	R/W
3.51.15:0	Code[31:16]	The two middle octets of the aggregation discovery code	R/W
3.52.15:0	Code[15:0]	The two least significant octets of the aggregation discovery code	R/W