IEEE 802.3
Call for Interest
Pin Optimized PHY Interface
Closing Report

IEEE 802.3 Closing Plenary

Jason Potterf (Cisco)

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CFI Request at 802.3 Opening Plenary, November 10, 2024

This is a call for interest to initiate a Study Group to develop a PAR and CSD for an Ethernet Media Independent Interface (MII) optimized for an exposed interconnect, e.g., chip-to-chip. The growing body of IEEE 802.3 Copper PHY standards that operate at lower speeds has intensified the demand for a modern, optimized MII. Application of PHYs such as 10BASE-T1L, 10BASE-T1S, proposed 100BASE-T1L, proposed 10BASE-T1M, and potentially future PHYs would see benefit in both single and multi-port implementations. Such an effort may afford reduced pin count and implementation complexity while enabling data for multiple ports on a single interface and support for features such as PHY-Level Collision Avoidance (PLCA). Most importantly, it could provide a modern alternative interface for PHYs that would otherwise use various industry specifications not currently in IEEE Std 802.3.

Motivation Overview

802.3dg 100 Mbps Long-Reach Single Pair Ethernet Benefits

- 802.3dg should provide a modern single-port solution for 100 Mbps data rates
  - SPI solution for 10 Mbps no longer works at 100 Mbps
  - Three-Pin PMD interface also is problematic at 100 Mbps
- Switch implementations desperately need a simpler multi-port solution
  - Existing multi-port MII solutions require a 10 Gbps SerDes which is overly complex

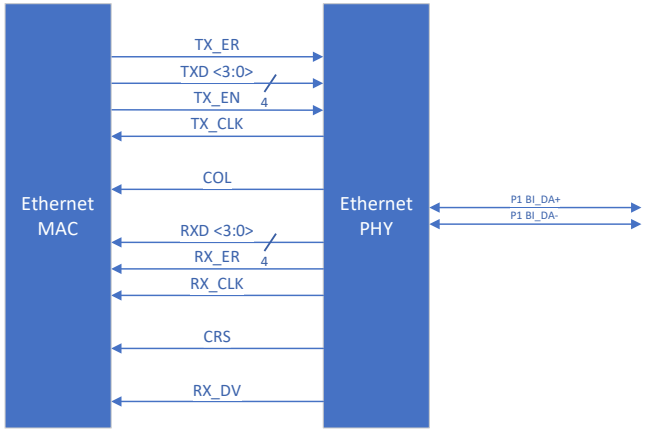
802.3da 10 Mbps Single Pair Multidrop Segments Enhancement Benefits

- PLCA over MII presents implementation challenges
- Multi-port MII solutions requiring a 10 Gbps SerDes are even less appropriate for 10 Mbps PHY implementations

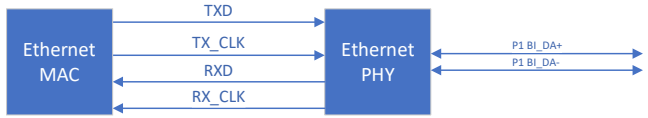
Asymmetric PHY projects could benefit from a reduced pin count solution with adaptive rates

What are we talking about?

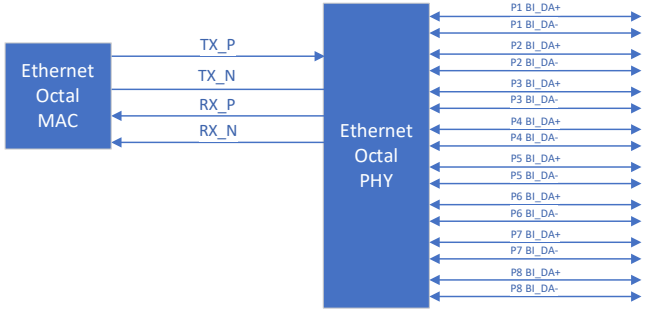
IEEE 802.3 MII
MII:MDI Ratio = 8:1



Potential Single-Port MII
MII:MDI Ratio = 2:1



Potential Multi-Port MII
MII:MDI Ratio = 1:4



Goal: Enable efficient, adoptable SPE implementations

A reduced pin count chip-to-chip MII provides more value per IC package pin than an MII-based solution, reducing implementation complexity and encouraging adoption

Why Now?

- PHY interconnect complexity for switches is hindering adoption
- Available MII interfaces prevent efficient implementation of 802.3cg 10-BaseT1S and 10-BaseT1L switches
- Octal PHY Implementation Options for 80 Mbit/s total bandwidth
  - MII – 16 pins / port x 8 ports + 2 Mgmt = ***130 Pins***
  - RMII – 8 pins / port x 8 ports + 2 Mgmt = ***66 Pins***
  - SGMII – 32 pins + 2 Mgmt = 34 pins and ***eight 1 Gbps SerDes***!
  - USGMII – 4 pins + 2 Mgmt = 6 pins, but requires a ***10 Gbps SerDes***!
- A Pin Optimized PHY Interface could accelerate SPE adoption

Supporters

- Tim Baggett – Microchip Technology
- Amir Bar-Niv – Marvell
- TJ Houck – Marvell
- Chad Jones – Cisco
- Peter Jones – Cisco
- Ragnar Jonsson – Marvell
- Jon Lewis – Dell Technologies
- Brett McClellan - Marvell
- Brian Murray – Analog Devices
- Alireza Razavi - Marvell
- Mehmet Tazebay - Broadcom
- Max Turner – Ethernovia
- Bob Voss – Panduit
- Peter Wu - Marvell
- George Zimmerman – CME Consulting / ADI, APL Group, Cisco, Marvell, OnSemi, Sony, SenTekse

CFI Consensus Building Meeting

- CFI Presentation: https://www.ieee802.org/3/cfi/1124_1/CFI_01_1124.pdf
  - Held Tuesday, November 12, 2024
  - Attendance: 50 Total (22 in room + 28 online)
- Straw Poll Results:
  - Should a study group be formed to develop a PAR, CSD responses, and objectives for “Pin Optimized PHY Interface”?
    - Y:22 N:0 A:4
  - Would you participate in the "Pin Optimized PHY Interface" Study Group in IEEE 802.3?
    - Y:17 N:4 A:7
  - Do you believe your affiliation would support your participation in the "Pin Optimized PHY Interface" Study Group in IEEE 802.3?
    - Y:18 N:2 A:7

Study Group Motion

Move that the IEEE 802.3 Working Group request the formation of a Study Group to develop a Project Authorization Request (PAR) and Criteria for Standards Development (CSD) responses for an Ethernet Media Independent Interface (MII) optimized for an exposed interconnect.

M: Jason Potterf – Cisco

S: Brian Murray – Analog Devices

Questions?

Thank you all!