IEEE 802.3
Call for Interest
Pin Optimized PHY Interface
Opening Report

IEEE 802.3 Opening Plenary

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CFI Announcement

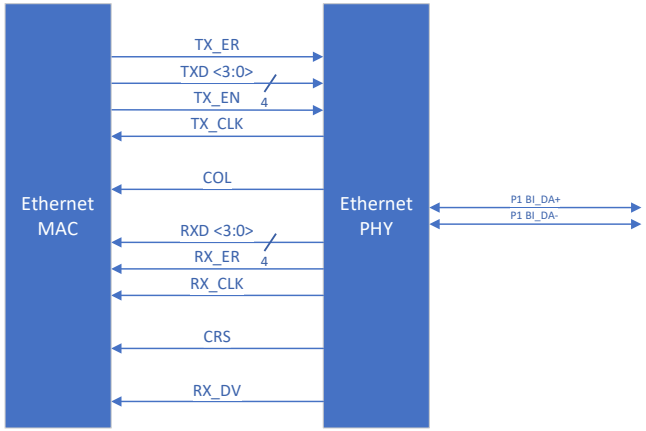
This is a call for interest to initiate a Study Group to develop a PAR and CSD for an Ethernet Media Independent Interface (MII) optimized for an exposed interconnect, e.g., chip-to-chip. The growing body of IEEE 802.3 Copper PHY standards that operate at lower speeds has intensified the demand for a modern, optimized MII. Application of PHYs such as 10BASE-T1L, 10BASE-T1S, proposed 100BASE-T1L, proposed 10BASE-T1M, and potentially future PHYs would see benefit in both single and multi-port implementations. Such an effort may afford reduced pin count and implementation complexity while enabling data for multiple ports on a single interface and support for features such as PHY-Level Collision Avoidance (PLCA). Most importantly, it could provide a modern alternative interface for PHYs that would otherwise use various industry specifications not currently in IEEE Std 802.3.

Motivation Overview

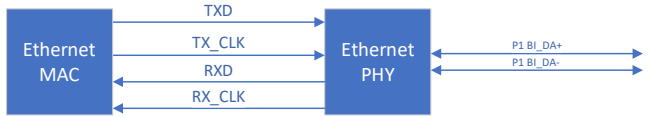
- 802.3dg 100 Mb/s Long-Reach Single Pair Ethernet Benefits
  - 802.3dg should provide a modern single-port solution for 100 Mbit/s data rates
    - SPI solution for 10 Mbits no longer works at 100 Mbit
  - Switch implementations desperately need a simpler multi-port solution
    - Existing multi-port MII solutions require a 10 Gbit/s SerDes which is overly complex
- 802.3da and 10BASE-T1S 10 Mb/s Single Pair Multidrop Benefits
  - PLCA over MII presents implementation challenges
  - Multi-port MII solutions requiring a 10 Gbit/s SerDes are even less appropriate for 10 MB/s PHY implementations
- Asymmetric PHY projects could benefit from a reduced pin count solution with adaptive rates

What are we talking about?

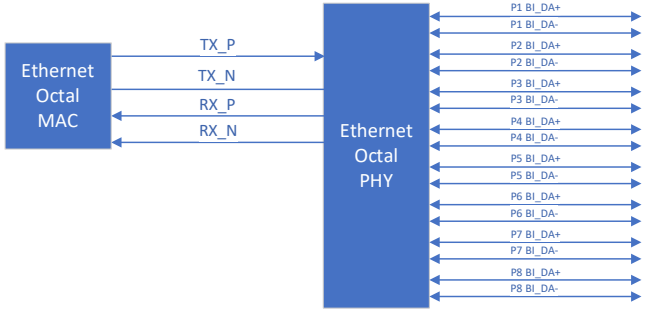
IEEE 802.3 MII
MII:MDI Ratio = 8:1



Potential Single-Port MII
MII:MDI Ratio = 2:1



Potential Multi-Port MII
MII:MDI Ratio = 1:4



Goal: Enable efficient, adoptable SPE implementations

A reduced pin count chip-to-chip MII provides more value per IC package pin than an MII-based solution, reducing implementation complexity and encouraging adoption

Why Now?

- PHY interconnect complexity for switches is hindering adoption
- Available MII interfaces prevent efficient implementation of 802.3cg 10-BaseT1S and 10-BaseT1L switches
- Octal PHY Implementation Options for 80 Mbit/s total bandwidth
  - MII – 16 pins / port x 8 ports + 2 Mgmt = ***130 Pins***
  - RMII – 8 pins / port x 8 ports + 2 Mgmt = ***66 Pins***
  - SGMII – 32 pins + 2 Mgmt = 34 pins and ***eight 1 Gbps SerDes***!
  - USGMII – 4 pins + 2 Mgmt = 6 pins, but requires a ***10 Gbps SerDes***!
- A Pin Optimized PHY Interface could accelerate SPE adoption

Logistics

A consensus building session will be held tomorrow night:

Date: Tuesday, November 12, 2024

Time: 19:00 – 20:30 Pacific Standard Time

Location: Regency E - Convention Level, 3rd Floor

CFI Announcement:
https://grouper.ieee.org/groups/802/3/cfi/request_1124_1.html

The vote to determine if a Study Group will be formed will take place at the IEEE 802.3 Closing Plenary on the afternoon of Thursday 14th November.

Questions?

Thank you all!