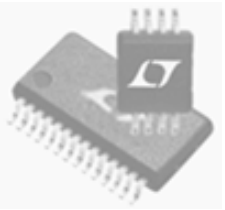
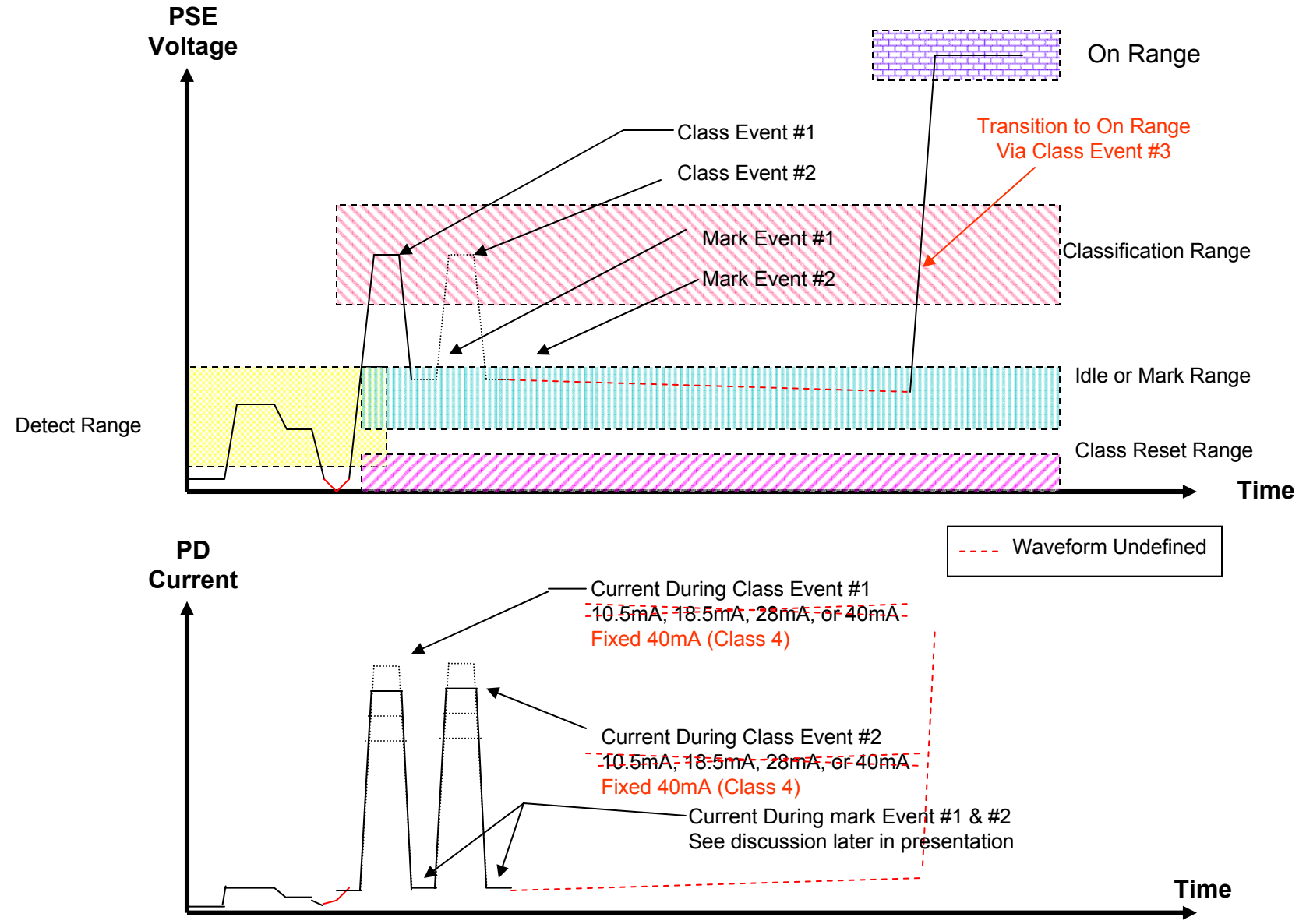


PoE Plus
IEEE 802.3at
Classification Ad Hoc
Extended Classification Using Two Classification Events

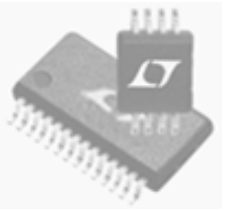
Clay Stanford
Linear Technology

December12 , 2006
Ad Hoc Meeting

802.3at Classification Using Two Classification Events



PoEP: IEEE 802.3at
2 Event Rules



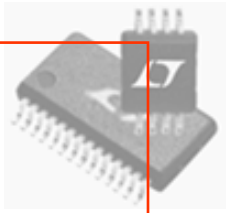
Type II (.at) PD Rules:

- PD is behind diode bridge so fall time is controlled by internal PD circuits and not PSE port voltage. Therefore a Type II (.at) PD is required to pull the internal supply down using the classification event current until the PD detects the Mark event. Once the PD has detected the Mark, the PD can stop pulling down on the port. Note that in this scenario, the port voltage may not discharge all the way down to the Mark range and this is not a problem.
- If the port voltage goes to reset range, PD state engine is reset and the PD will go to the detect state.
- During Mark event, Type II (.at) PD R≠25Kohm, to avoid .af PSE classing again.

Type II (.at) System Rules:

- Type II (.at) PSE is the master, generating port voltage. Type II (.at) PD is slaved to Type II (.at) PSE , responding with port current.
- System is designed so that Type II (.at) PD spends a limited amount of time in the Mark range in case Type II (.at) PD is using dynamic memory which requires power to maintain state.
- Type II (.at) PSE must transition from 2nd Mark event to Power On without going down into Reset range.

PoEP: IEEE 802.3at
2-Event Type I/II (.af/.at) Interaction



Type II (.at) PSE with Type I (.af) PD:

- If Type II (.at) PSE sees 0-0, 1-1, 2-2, 3-3, or 4-4, it assumes Type I (.af) PD and powers per .af spec, i.e. 15.4W, 4W, 7W, 15.4W, or 15.4W respectively.
- Type I(.af) PD that uses class 4 (in error) may get powered with 30W if Type II(.at) PSE. OK
- If PSE sees class 1,2, or ~~3, it can either ping twice or just once.~~ We don't care.

Type II (.at) PSE with Type II (.at) PD:

- If Type II (.at) PSE sees ~~changing class values (i.e. 1-2, 1-3,~~ etc)4-4, it knows PD is a Type II (.at) PD.

.Type I (.af) PSE with Type II (.at) PD:

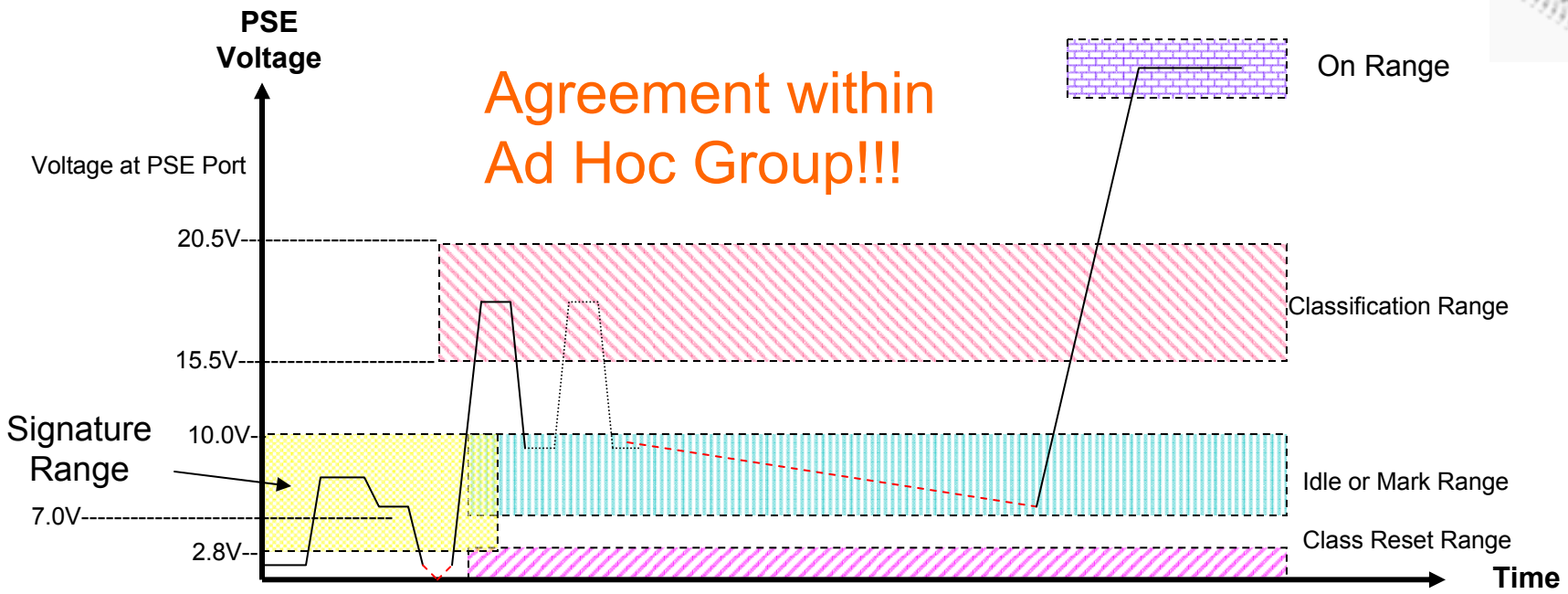
- ~~If Type I (.af) PSE sees Type II (.at) PD, it will use first class. Therefore, new 2W Type II (.at) PD should use class 1-x, so that Type I (.af) PSE allocates 4W. Similarly, new 11W Type II (.at) PD should use 3-x so that Type I (.af) PSE allocates 15.4W.~~

No more 2W or 11W PDs using layer 1.

Comments

- Type I (.af) PD may not pull internal PD supply down quickly between pulses but it doesn't matter. With the Mark event in the Signature range, Type I (.af) PD might "float" at some voltage 10-15.5V, but will return to class range when PSE drives port back to class voltage.
- Class 0 is not used by Type II (.at) PD because Class 0 can be 0mA and would not pull port low. Port needs to be pulled low by Type II (.at) PD so that Type II (.at) PD can see that Type II (.at) PSE has driven classification voltage to the Mark event.

Voltage Ranges and Timing Specification



PSE VOLTAGE SPECIFICATIONS		
FUNCTION	MIN (V)	MAX (V)
Classification (at PSE)	15.5	20.5
Mark (at PSE)	7.0	10
Reset Low	0	2.8
Reset High	**	

**Reset occurs when PD passes UVLO falling threshold

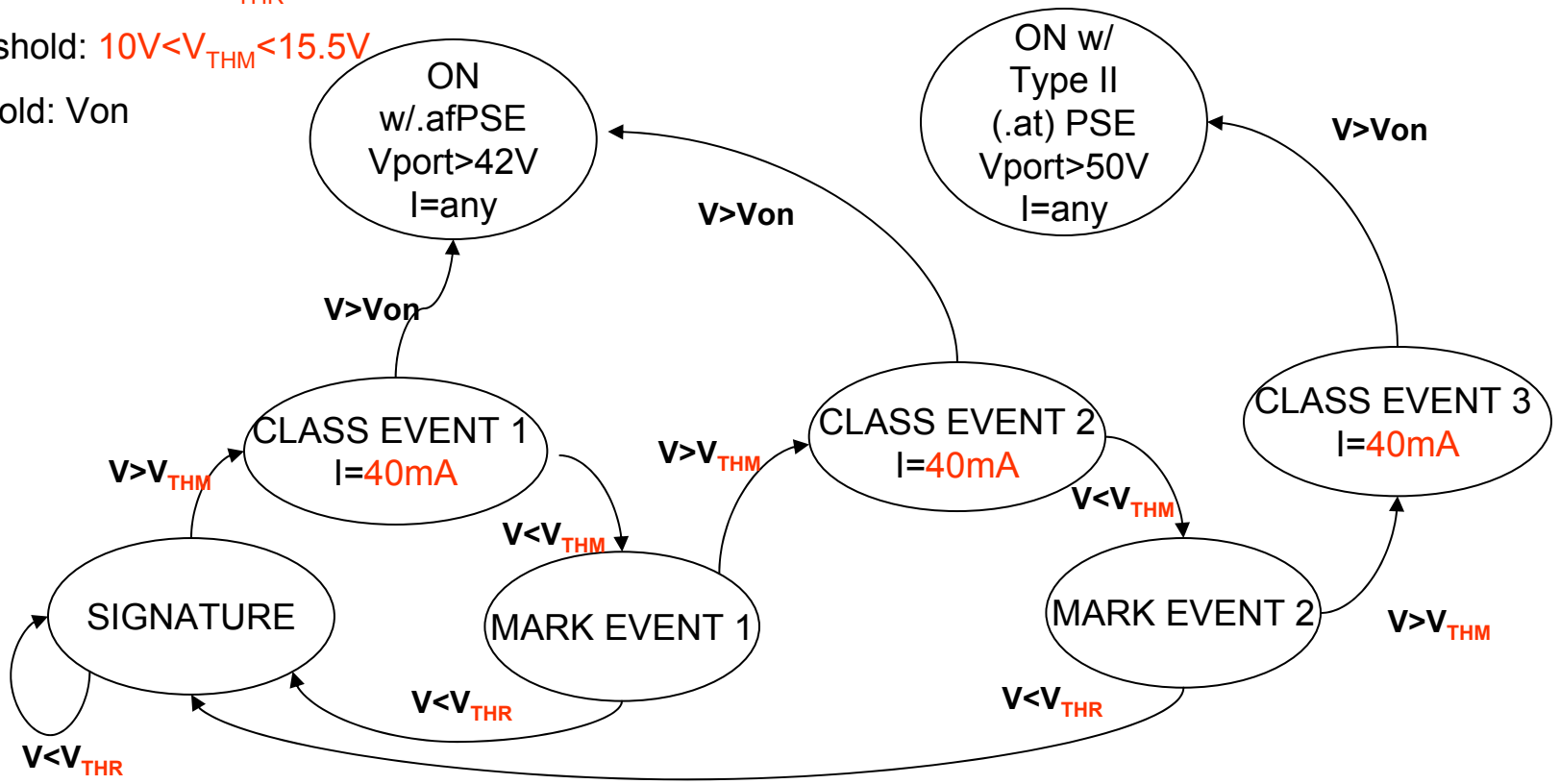
TIMING SPECIFICATIONS		
EVENT	MIN (ms)	MAX (ms)
1st Class	20	30
1st Mark	2	4
2nd Class	10	18
2nd Mark	2	*
TOTAL	34ms	~400ms

*Time from end of detection until power on is limited. See 33.2.8.13

3-Event Classification State Engine in PD

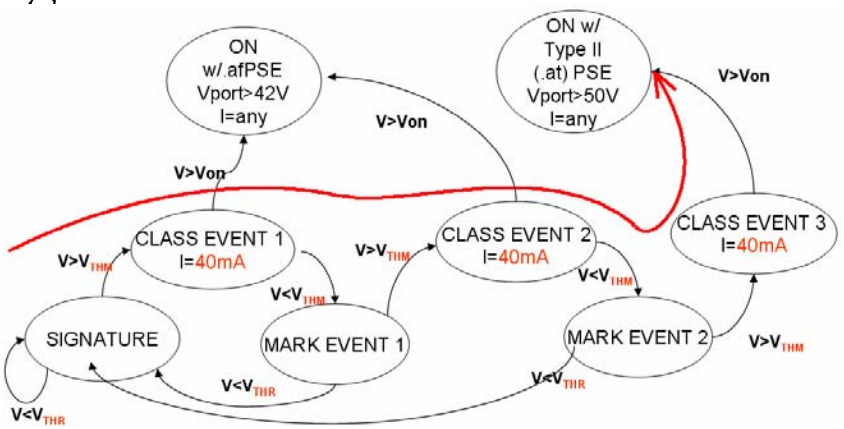
Three Thresholds Associated with Method

- Reset Threshold: $2.8V \leq V_{THR} < 7.0V$
- Mark Threshold: $10V < V_{THM} < 15.5V$
- On Threshold: Von



PD Behavior During Mark Event

- PD not to present 25Kohm during mark to address non-compliant PSE
- Range of PD current limited to ease PSE design task



~~PROPOSED~~ PD MARK SPECIFICATION

- PD 2-point signature to be:

  R_{PD} < 15Kohm or R_{PD} > 33Kohm

- PD current to be:

  0.5mA < I_{PD} < 2.0 mA