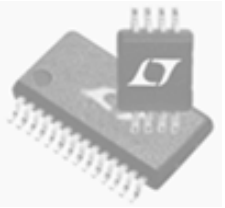
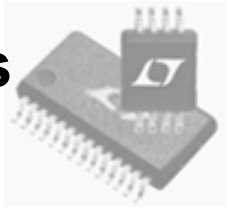


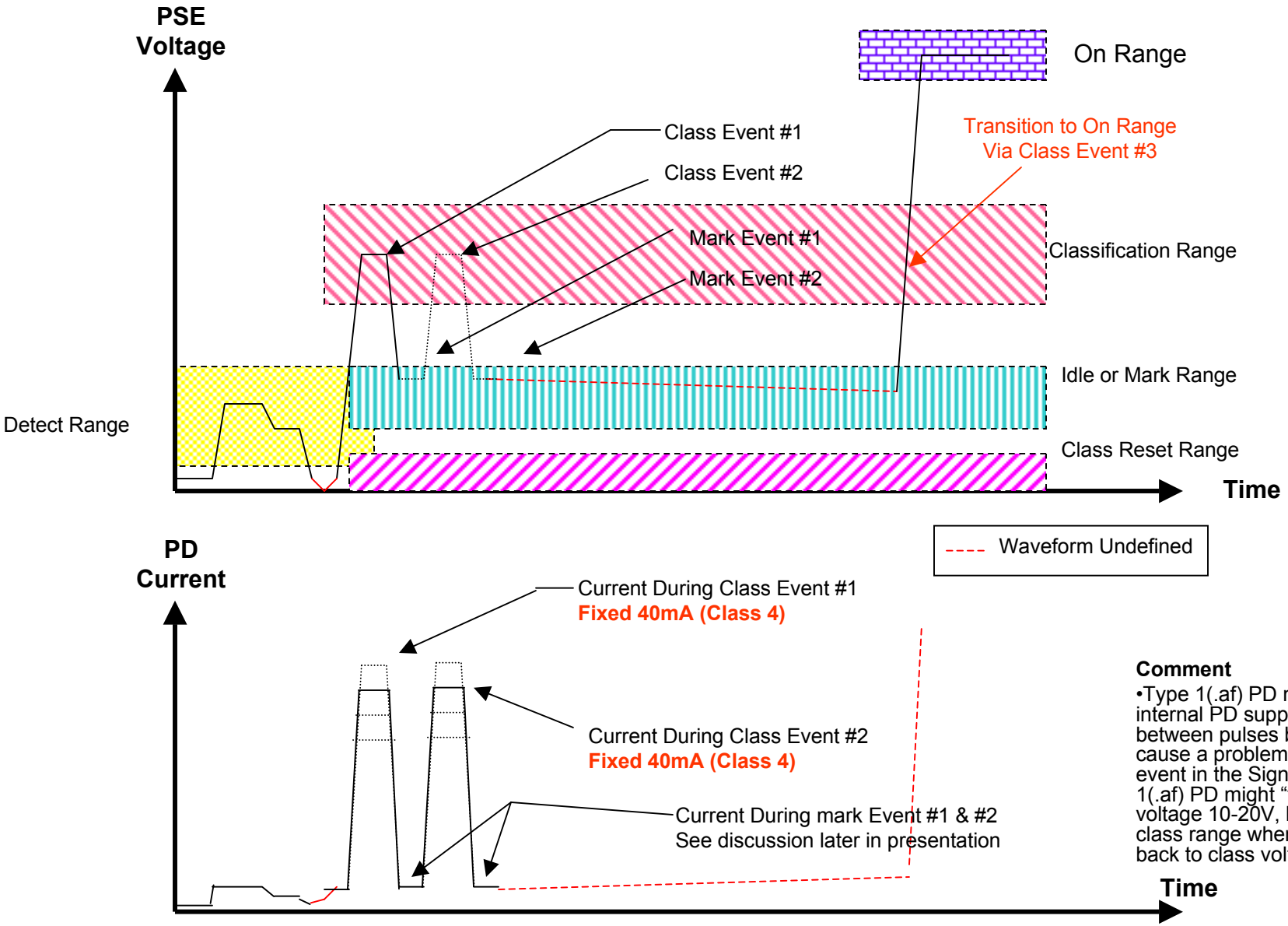
PoE Plus
IEEE 802.3at
Classification Ad Hoc
Extended Classification Using Two Classification Events

Clay Stanford
Linear Technology

January 17, 2007
Monterey

802.3at Classification Using Two Classification Events

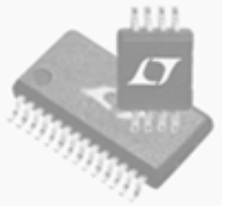




Comment

•Type 1(.af) PD may not pull internal PD supply down quickly between pulses but this doesn't cause a problem. With the Mark event in the Signature range, Type 1(.af) PD might "float" at some voltage 10-20V, but will return to class range when PSE drives port back to class voltage.

PoEP: IEEE 802.3at
Two Event Rules



Type 2 (.at) PD Rules:

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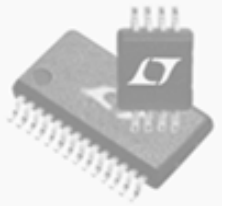
- If the port voltage goes to reset range, PD state engine is reset and the PD will go to the detect state.

Type 2 (.at) System Rules:

- Type 2 (.at) PSE is the master, generating port voltage. Type 2 (.at) PD is slaved to Type 2 (.at) PSE , responding with port current.
- System is designed so that Type 2 (.at) PD spends a limited amount of time in the Mark range in case Type 2 (.at) PD is using dynamic memory which requires power to maintain state.
- Type 2 (.at) PSE must transition from 2nd event through Class Event 3 to Power On without going down into Reset range.

PoEP: IEEE 802.3at
Two-Event Type 1/2 (.af/.at) Interaction



Type 2 (.at) PSE with Type 1 (.af) PD:

- If a Type 2(.at) PSE sees class 0, 1, 2, or 3, it assumes Type 1(.af) PD and powers per .af spec, i.e. 15.4W, 4W, 7W, 15.4W respectively.
  - Note: Type 1(.af) PD that uses class 4 (in error) will get powered with 30W by a Type 2(.at) PSE. This is a minor annoyance with this class scheme and is considered acceptable.
  - If a Type 2(.at) PSE sees class 4, and it is using layer 1 only for classification, it must ping twice.
  - If a Type 2(.at) PSE sees class 0,1,2, or 3, it has the option of pinging either one or two times.

May06 motion to include 2W class and July06 motion for ~9W class will not be supported.

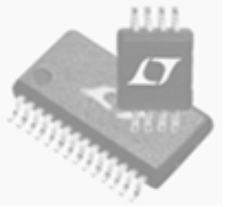
Type 2(.at) PSE with Type 2(.at) PD:

- Type 2(.at) PSEs should see class 4 when connected to a Type 2(.at) PD.
- Type2(.at) PSE only using L1 will ping twice to signal to the Type 2(.at) PD that it is a Type 2 PSE.
- If a Type 2(.at) PSE sees inconsistent class results (i.e. 4-1, 4-2, etc), the behavior is non-compliant and PSE action is undefined.

.Type 1 (.af) PSE with Type 2 (.at) PD:

- If a Type 1(.af) PSE sees a Type 2 (.at) PD, it will see class 4 and power at 15.4W.

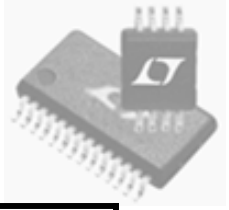
Motion from March 2006



The IEEE 802.3at Task Force affirms that a PD requiring more than 12.95W will support a Layer-1 Classification extension and a Layer-2 Classification mechanism.

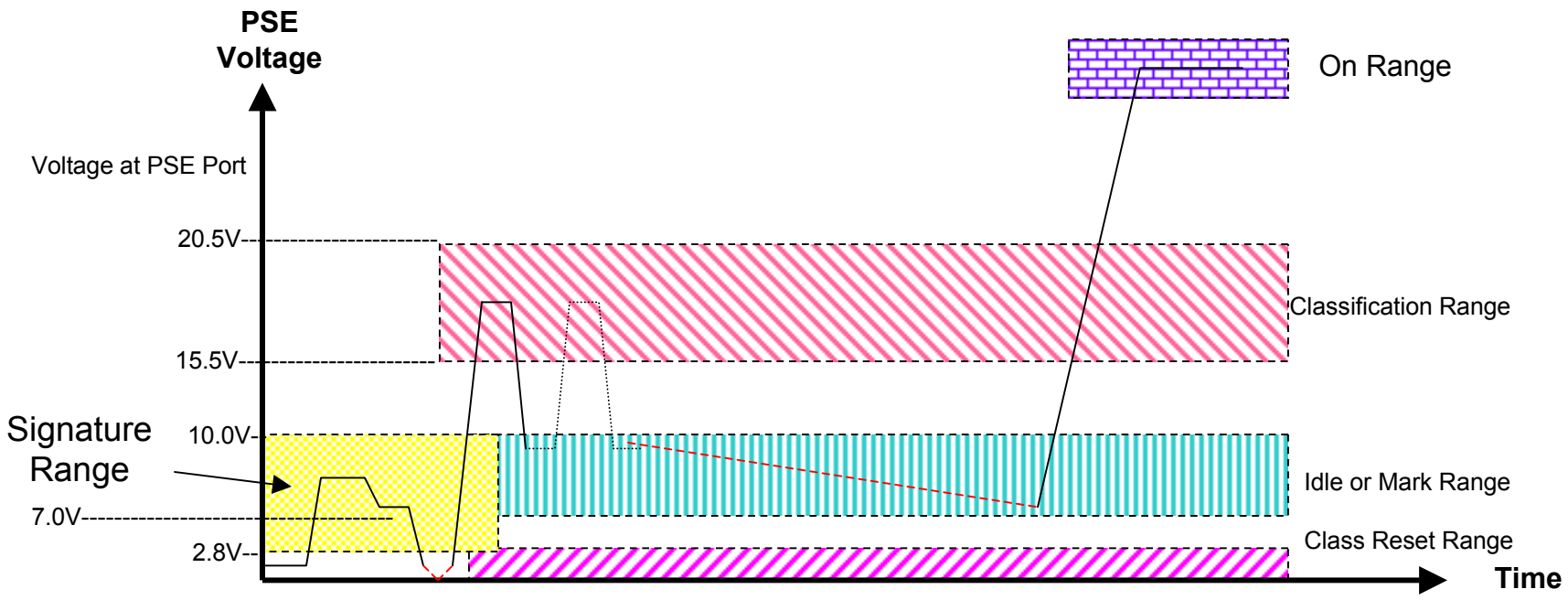
Endpoint PSEs must support Layer-2 classification or Layer-1 classification extension for PDs requiring more than 12.95W.

All Possible PSE/PD Combinations

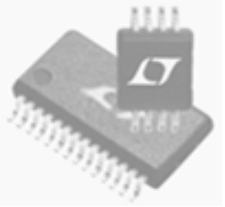


PSE TYPE	PD TYPE	COMMENTS
Type 1(.af)	Type 1(.af)	Existing 802.3af system, class 0, 1, 2, or 3.
Type 1(.af)	Type 2(.at)	Type 1(.af)PSE sees class 4 and powers per 802.3af specification, i.e. 15.4W. Type 2(.at) PD can only assume Type 1 PSE and must operate with 15.4W and alert user not enough power.
Type 2(.at) L1 i.e. high power midspan	Type 1(.af)	Type 2(.at) PSE sees class 0, 1, 2, 3 and powers per 802.3af specification.
Type 2(.at) L1 i.e. high power midspan	Type 2(.at)	Type 2(.at) PSE sees class 4 and powers with maximum allowable 802.3at power level. Type 2(.at) PD sees two class pings and knows Type 2 PSE connected. Power information is known before PD is powered.
Type 2(.at) L2 i.e. end point PSE	Type 1(.af)	Type 2(.at) PSE sees class 0, 1, 2, 3 and powers per 802.3af specification. Layer 2 communication fails to establish. Power level is maintained at .af levels. PD sees af behavior and operates under .af specs.
Type 2(.at) L2 i.e. end point PSE	Type 2(.at)	Type 2(.at) PSE sees class 4 and powers with 15.4W. Layer 2 communication is established and mutual identification is established. High power operation begins.

Voltage Ranges and Timing Specification



PSE and PD Voltage Ranges

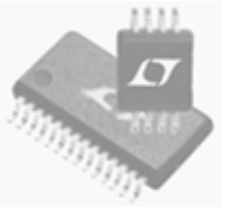


PSE VOLTAGE SPECIFICATIONS		
FUNCTION	MIN (V)	MAX(V)
Classification	15.5[1]	20.5[1]
Mark	7.0	10
Low Reset Range	0	2.8[1]
High Reset Range	--	--

PD VOLTAGE SPECIFICATIONS		
FUNCTION	MIN (V)	MAX(V)
Classification	14.5[1]	20.5[1]
Mark	6.9[2]	10[3]
Low Reset Range	0	2.8[3]
High Reset Range	30[1,4]	

Notes on Calculations

1. Value from 802.3af specification.
2. Assume cable max resistance = 20ohms so as to also work with .af systems.
   Cable drop max = 2mA (mark current max) * 20ohms = .04V~=0.1V.
   With 7V at PSE, may only be ~6.9V at PD.
3. PD Mark and Reset limits are not equivalent to PD signature range (2.7V-10.1V). PD upper limits are equal to PSE upper limits.
4. Reset high occurs when powered PD drops below PD power supply turn off voltage.



Timing Specification

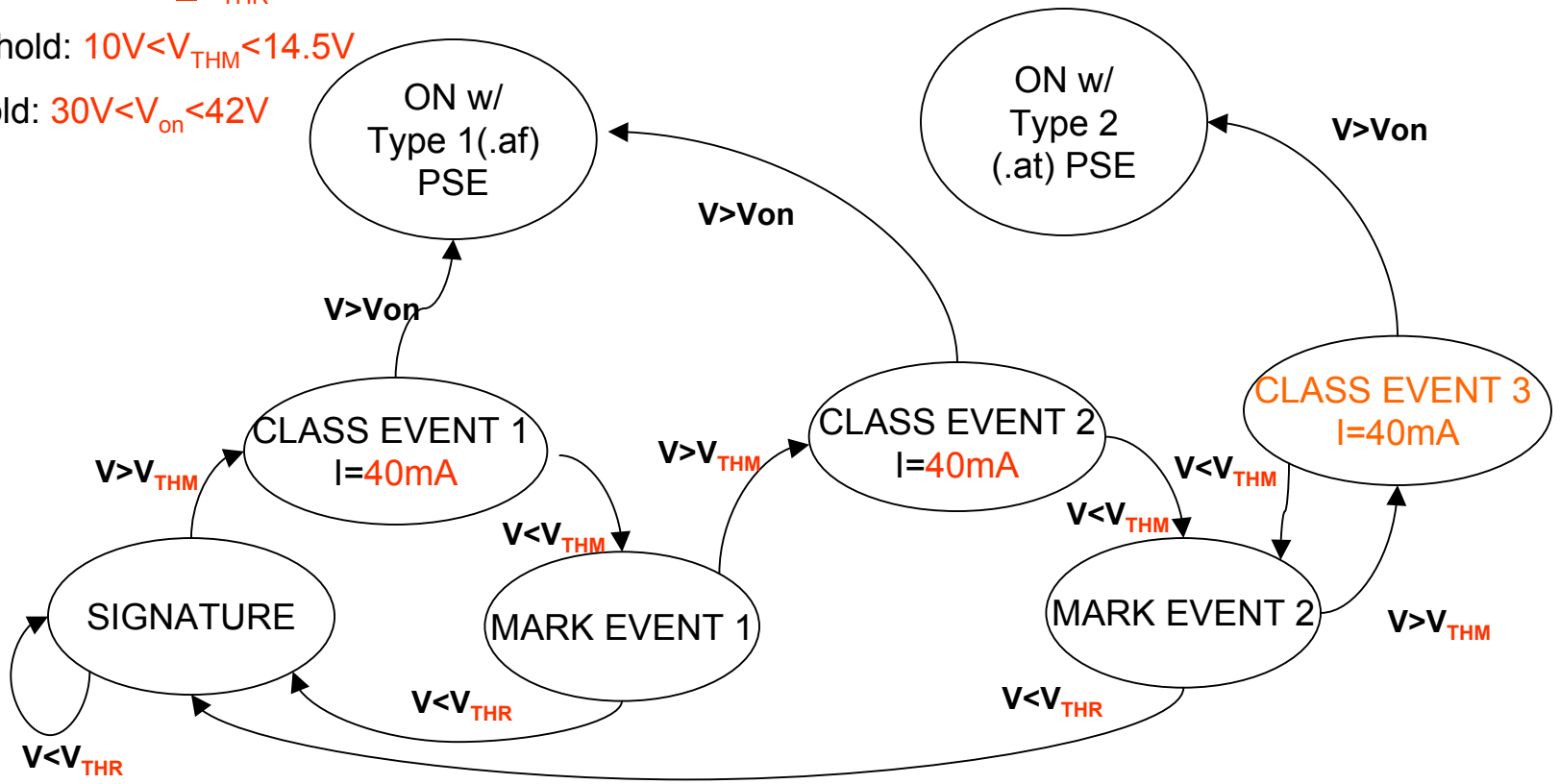
TIMING SPECIFICATIONS		
EVENT	MIN (ms)	MAX (ms)
1st Class	20	30
1st Mark	2	4
2nd Class	10	18
2nd Mark	2	Note 1
TOTAL (for reference only)	34ms	~400ms

Note 1. Time from end of detection until power on is limited by section 33.2.8.13.

Classification State Engine in PD

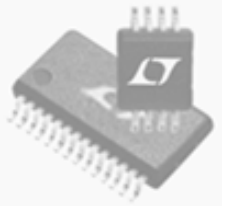
Three Thresholds Associated with Method

- Reset Threshold: $2.8V \leq V_{THR} < 6.9V$
- Mark Threshold: $10V < V_{THM} < 14.5V$
- On Threshold: $30V < V_{on} < 42V$



Class Event 3 exists to create a defined behavior for Type 2(.at) PDs when pinged repeatedly. This allows future expansion of the classification mechanism with a known response from Type 2(.at) PDs. PD transitions through Class Event 3 during power on.

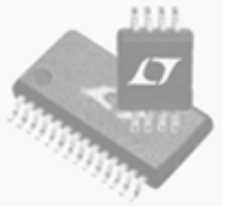
PD Behavior During Mark Event



PD current to be: $0.25mA < I_{PD} < 2.0\ mA$

- Limiting range of PD current during Mark state eases PSE requirements.

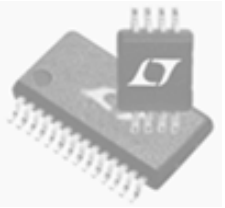
Redlines



The Schindler/Diab Motion from Dallas (11/06) significantly changed the Two-Event classification mechanism.

The following slides include redlines to document the change that occurred when the Schindler/Diab Motion was passed.

PoEP: IEEE 802.3at
Two Event Rules



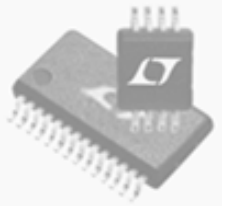
Type 2 (.at) PD Rules:

- PD is behind diode bridge so fall time is controlled by internal PD circuits and not PSE port voltage. Therefore a Type 2 (.at) PD is required to pull the internal supply down using the classification event current until the PD detects the Mark event. Once the PD has detected the Mark, the PD can stop pulling down on the port. Note that in this scenario, the port voltage may not discharge all the way down to the Mark range and this is not a problem.
- If the port voltage goes to reset range, PD state engine is reset and the PD will go to the detect state.
- During Mark event, Type 2 (.at) PD R≠25Kohm, to avoid .af PSE classing again.

Type 2 (.at) System Rules:

- Type 2 (.at) PSE is the master, generating port voltage. Type 2 (.at) PD is slaved to Type 2 (.at) PSE , responding with port current.
- System is designed so that Type 2 (.at) PD spends a limited amount of time in the Mark range in case Type 2 (.at) PD is using dynamic memory which requires power to maintain state.
- Type 2 (.at) PSE must transition from 2nd Mark event to Power On without going down into Reset range.

PoEP: IEEE 802.3at
Two-Event Type 1/2 (.af/.at) Interaction



Type 2 (.at) PSE with Type 1 (.af) PD:

- If Type 2 (.at) PSE sees 0-0, 1-1, 2-2, 3-3, ~~or 4-4,~~ it assumes Type 1 (.af) PD and powers per .af spec, i.e. 15.4W, 4W, 7W, ~~15.4W, or 15.4W~~ respectively.
- Type 1(.af) PD that uses class 4 (in error) will get powered with 30W by a Type 2(.at) PSE. This is a minor annoyance with this class scheme and is considered acceptable.
- If a Type 2(.at) PSE sees class 0,1,2, or 3, it has the option of pinging either one or two times. If a Type 2(.at) PSE sees class 4, and it is using layer 1 only for classification, it must ping twice.

Type 2 (.at) PSE with Type 2 (.at) PD:

- If Type 2 (.at) PSE sees ~~changing class values (i.e. 1-2, 1-3, etc)~~, class 4 it assumes PD is a Type 2 (.at) PD.

.Type 1 (.af) PSE with Type 2 (.at) PD:

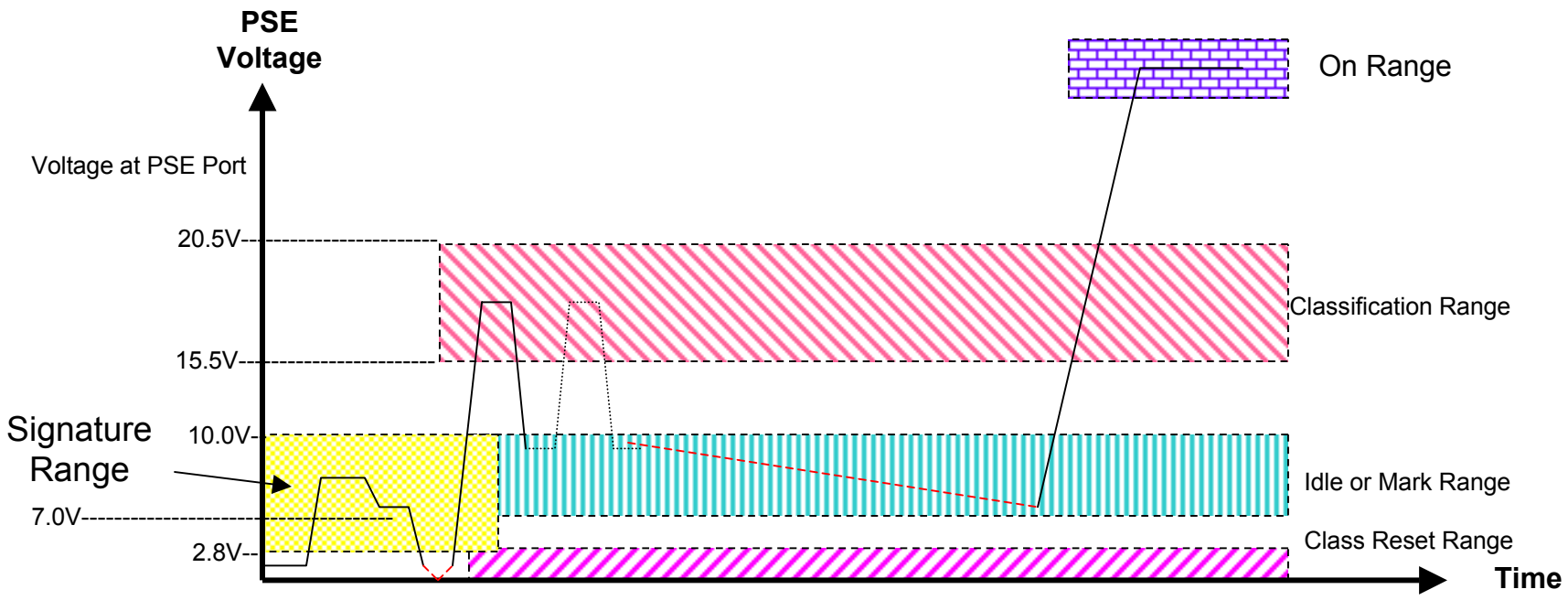
- ~~If Type 1 (.af) PSE sees Type 2 (.at) PD, it will use first class. Therefore, new 2W Type 2 (.at) PD should use class 1-x, so that Type 1 (.af) PSE allocates 4W. Similarly, new 11W Type 2 (.at) PD should use 3-x so that Type 1 (.af) PSE allocates~~ 15.4W.

Just gets powered with 15W. No more 2W or 11W PDs using layer 1.

Comments

- Type 1 (.af) PD may not pull internal PD supply down quickly between pulses but it doesn't matter. With the Mark event in the Signature range, Type 1 (.af) PD might "float" at some voltage 10-15.5V, but will return to class range when PSE drives port back to class voltage.
- Class 0 is not used by Type 2 (.at) PD because Class 0 can be 0mA and would not pull port low. Port needs to be pulled low by Type 2 (.at) PD so that Type 2 (.at) PD can see that Type 2 (.at) PSE has driven classification voltage to the Mark event.

Voltage Ranges and Timing Specification



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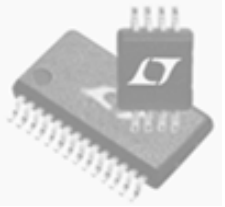

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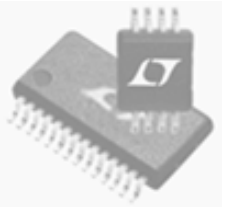

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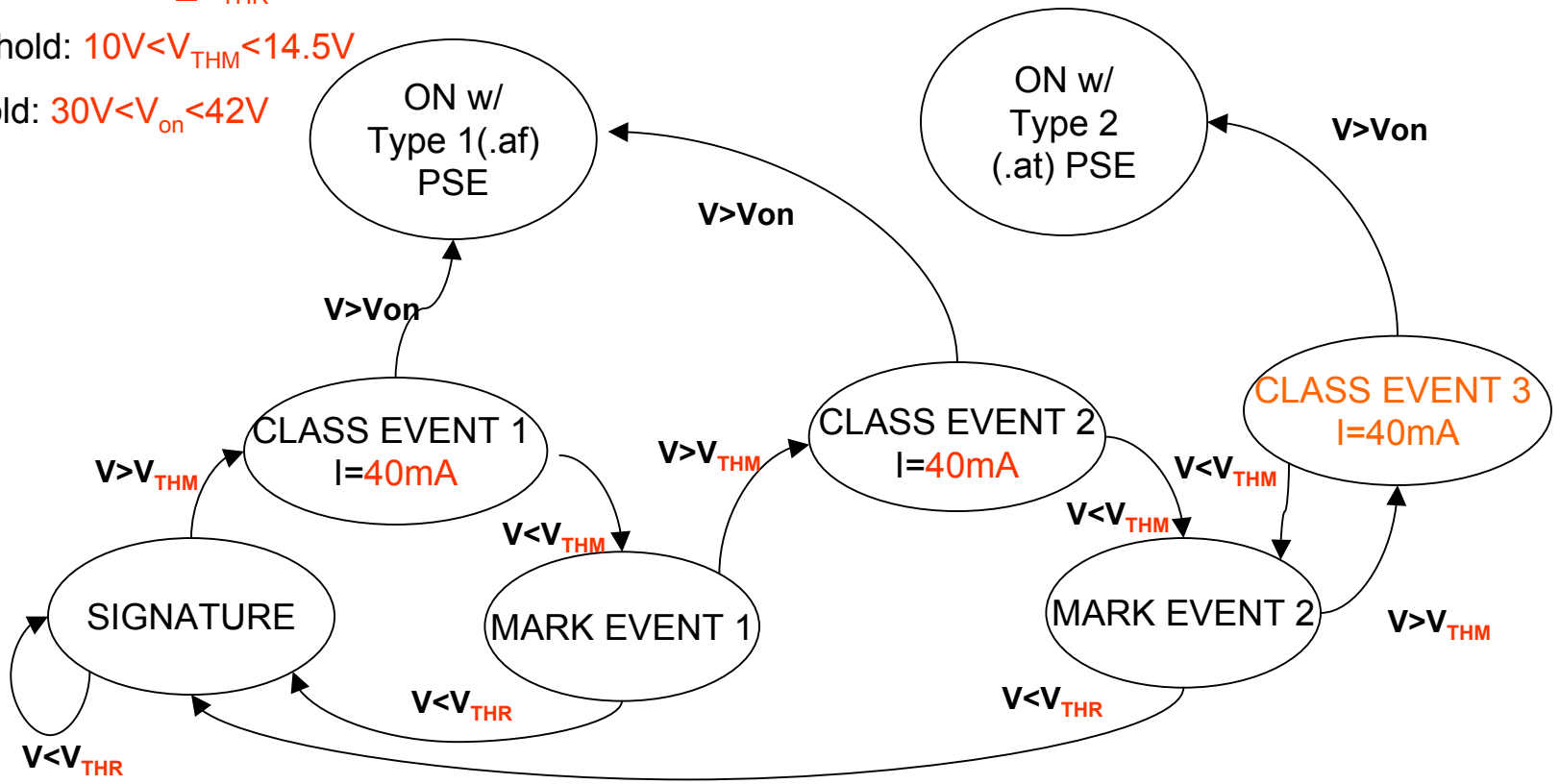

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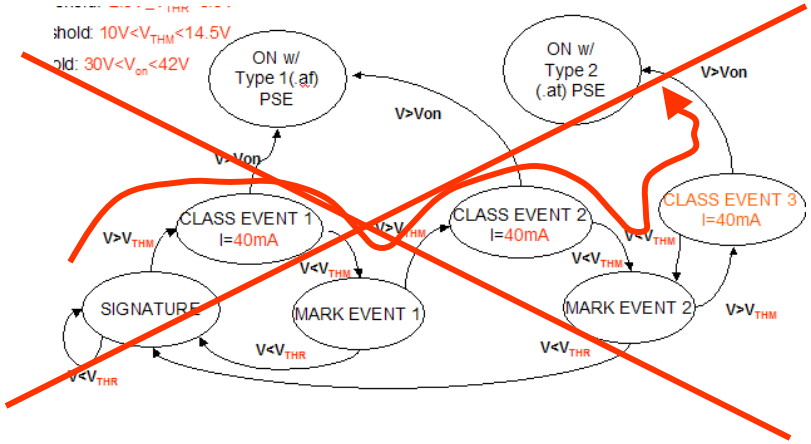
PD Behavior During Mark Event

- ~~PD not to present 25Kohm during mark to address non-compliant PSE~~
- Range of PD current limited to ease PSE design task



PD MARK MODE SPECIFICATION

- ~~PD 2-point signature to be:~~

  ~~R_{PD} < 15Kohm or R_{PD} > 33Kohm~~

- PD current to be:

  0.25mA < I_{PD} < 2.0 mA