PoE Plus
IEEE 802.3at
Classification Ad Hoc

Resolving Draft 1.0
Comments in L1 Bucket

Clay Stanford
Linear Technology
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Teleconference

Cl 33 SC 3.4.2 P 57 L 38 # 255

Stanford, Clay Linear Technology

Comment Type E *Comment Status* D *L1 adhoc*

Define Mark Event Voltage range. It will make text more clear.

Define Reset Voltage range. It will make text more clear.

Label Reset Threshold Vreset_th to be more consistant.

SuggestedRemedy

Table 33-11a

Item 2: Add "10" to max column.

Item 5: Change Symbol from Vreset to Vreset_th

Add new item 6, Classification Reset Voltage Vreset V 0(V) 2.8(V) See 33.3.4.2.1

Proposed Response *Response Status* O

see 256

Cl 33 SC 3.4.2.1 P 57 L 53 # 256

Stanford, Clay Linear Technology

Comment Type E *Comment Status* D *L1 adhoc*

Text will be more clear if we use Vmark range.

SuggestedRemedy

Line 53 IS:

When the voltage at the PI is between VMark min and VMark_th min, a Type 2 PD shall return a non-valid detection signature as defined in Table 33–9.

Line 53 SHOULD BE:
When the voltage at the PI is IN THE RANGE OF Vmark, a Type 2 PD shall return a non-valid detection signature as defined in Table 33–9.

Proposed Response *Response Status* O

see 255

Table 33–11a—2-Event Physical Layer classification electrical requirements

Item	Parameter	Symbol	Units	Min	Max	Additional Information
1	Class Event Voltage	V_{Class}	V	14.5	20.5	
2	Mark Event Voltage	V_{Mark}	V	6.9		
3	Mark Event Current	I_{Mark}	mA	0.25	2	See 33.3.4.2.1
4	Mark Event Threshold	V_{Mark_th}	V	10	14.5	See 33.3.4.2.1
5	Classification Reset Threshold	V_{Reset}	V	2.8	6.9	See 33.3.4.2.2

10V

Vreset_th

6 | Classification Reset Voltage | Vreset| V | 0 | 2.8 | See 33.3.4.2.1

Add this new entry

Cl 33 SC 2.7.2a P 38 L 40 # 83

Darshan, Yair — Microsemi Corporation

Comment Type TR *Comment Status* D *L1 adhoc*

Draft 1.0:
If after Iclass_lim event the PSE classify the PD as class 4, why we need to be in Reset range?
It looks that the text "Subsequent to such classification, the PSE shall ensure that the voltage at the PI enters the VReset range for at least TReset min as defined in Table 33-4a prior to powering the port." is not required.

SuggestedRemedy

Option a:
Classification ad hoc to explain why we need it.
If we don't need it, to delete it.

Option b:
Change the text to read:
"If PSE decides not to complete two event classification due to any reason, or decides to ignor classification results, the PSE shall ensure that the voltage at the PI enters the VReset range for at least TReset min as defined in Table 33-4a prior to powering the port."

Proposed Response *Response Status* O

←-This comment is OBE.
See 149 below. Sentence in question has been deleted.

Cl 33 SC 2.7.2a P 38 L 35 # 130

Schindler, Fred — Cisco Systems

Comment Type ER *Comment Status* D *L1 adhoc*

The text:
"… transition to the POWER_ON state without allowing the voltage at the PI to go below Vmark." Conflicts with text at L40: "… shall ensure the PI enters the Vreset range…" because Vmark > Vreset.

SuggestedRemedy

Have the L1 ad hoc provide text to correct this section.

Proposed Response *Response Status* O

defer to L1

←-This comment is OBE.
See 149 below. Sentence in question has been deleted.

If any measured IClass is equal to or greater than IClass_LIM min as defined in Table 33–4a, the PSE shall classify the PD as Class 04. If any measured IMark is greater than or equal to IMark_LIM min as defined in Table 33–4a, the PSE shall classify the PD as Class 0. **Subsequent to such classification, the PSE shall ensure that the voltage at the PI enters the VReset range for at least TReset min as definied in Table 33–4a prior to powering the port.**

2.7.2a P 38 L 41 # 149

STMicroelectronics

R *Comment Status* A

Iclass is greater than Iclass_lim, the assigned class is Class4. There is no he voltage at the PI in this case. Whithout this sentence, if the 2-event classification succeded, the PD will work correctly as class 4.
With a reset instead, the PD will work as a Type1 PD, wasting a lot of the allocated by the PSE.

SuggestedRemedy

Remove the sentence:
Subsequent to such classification, the PSE shall ensure that
the voltage at the PI enters the VReset range for at least TReset min as definied in Table 33–4a prior to powering the port.

Response *Response Status* C

ACCEPT.

Cl 33 SC 2.7.2a P 37 L 52 # 129

Schindler, Fred — Cisco Systems

Comment Type TR *Comment Status* A *L1 adhoc*

The same settling requirements for Type-1 classification should be imposed on Type-2 first class, classification. A Type 1 PD requires 5 ms to provide a valid class current (table 33-12, item 9). This comment also applies to p38 L24.

SuggestedRemedy

Have the L1 ad hoc review and correct this section.

Response *Response Status* C

ACCEPT IN PRINCIPLE.

The editor to apply the same transient settling timing to both 1-event and 2-event classifications. Page 37, line 43.

While on this subject, comment 245 was accepted and suggested aligning Type 1 and Type 2 class timing. However, editor instructions do not this state explicitly. Should we clarify both timings s to be 6ms?

Comment 243 corrected page 37, line 43.

Comment 129 suggests 1-Event and 2-Event 2 PSEs should have same time measurement delay requirement. We can add the same sentence for a Type 2 PSE at the end of p37:

Measurement of Iclass shall be taken afte 6ms to ignore initial transients.

This sentence could also be inserted at p38L27.

Note that I do not think the .af spec mentioned waiting a time before measuring. It was implied in the PSE timing of 10ms min while PD stability was speced at 5ms max.

Cl 33 SC 2.8 P 41 L 38 # 245

Stanford, Clay — Linear Technology

Comment Type T *Comment Status* A

When the 2-event classification was created, it was desired to perform it quickly so the PSE miniumum timing was reduced from 10ms to 6ms. (The PD must be stable within 5ms.) There now is a discrepancey beteeen 1-event and 2-event classification in this minimum pulse period. It would be best to align the two timing numbers.

Also, Table 33-5 entry would make more sense moved to table 33-4a

SuggestedRemedy

IS:
Table 33-5, item 20
10mS minimum.

SHOULD BE:
6ms minimum.

Move entire line over to Table 33-4a.

Response *Response Status* C

ACCEPT IN PRINCIPLE.

Change title of moved line from "Classification timing" to "1-Event class timing"

add a new column titled "1-Event/2-Event"
1a = 1&2 event
1b = 1&2 event
2a - 9 = 2 event
item 10 (the new item) = 1 event

Cl 33 SC 3.4.2 P 57 L 50 # 111

Darshan, Yair Microsemi Corporation

Comment Type T *Comment Status* D *L1 adhoc*

Draft 1.0:
PD don't have to present class 4 for infinite classification attempts.
Id adds thermal burden and costs.
In any case if system has problems it may initiate consecutive startups every Ted which is defined in Table 33-5 item 21.

SuggestedRemedy

To be added after line 50.
"PD may revert to IDLE state if PSE initiate more then 3 consecutive classification attempts within less then Ted as specified in Table 33-5."

Proposed Response *Response Status* O

defer to L1

A Type 2 PD shall return a Class 4 signature irrespective of the number of classification voltage probes performed by a PSE.

DISCUSS

Cl 33 SC 2.7.2a P 38 L 40 # 102

Darshan, Yair Microsemi Corporation

Comment Type TR *Comment Status* D *L1 adhoc*

Draft 1.0:

When PSE classify the PD after Icllas_LIM event it should get to Vreset for Treset prior to power the port.

In order to achieve this objective PD should consume some minimum current to allow PSE to reduce its port voltage due the capacitors in the channel.

SuggestedRemedy

The classification ad hoc to adress this issue if it is possible to implement i.e. to have I>>0 at 2.8V to 6.9 Volt range for Treset.

Proposed Response *Response Status* O

defer to L1

DISCUSS

Cl 33 SC 2.7 P 36 L 27 # 127

Schindler, Fred Cisco Systems

Comment Type TR *Comment Status* D *L1 adhoc*

The text:
"If a PSE successfully completes detection of a PD, but the PSE fails to complete classification of a PD, then a Type 1 PSE shall assign the PD to Class 0 and a Type 2 PSE shall assign the PD to class 4." imposes an unnecessary design requirement. This text also enables dump-Type 2 PDs that do not support DLL classification.

A system that does not provide a proper class is:
a) Experiencing a temporary fault that will rectify itself.
OR
b) Noncompliant.

A compliant Type-2 PD has not achieved mutual identification and will remain in type-1 power mode. Therefore, requiring class-4 power serves no legitimate purpose.

A PSE that classifies a PD and gets an invalid results is not probable because this occurs only when class current exceeds 51 mA.

SuggestedRemedy

Require PSEs that performs classification, to either repeat the detection and classification steps, or repeat the classification step, until legal responses are achieved.

Proposed Response *Response Status* O

defer to L1

DISCUSS

New Mark Timing Issue

- PSE Mark Event timing
  Table 33-4a, item 4
  (D1.0, page 39, line 19)
- Though hardware will interoperate, port loading during event will effect observable timing behavior.
- Timing start and stop points are not clearly defined in standard.
- Intent was for timing event to commence when PSE starts driving port with Mark Event Voltage.
- Intent was for timing event to end when PSE stops driving port with Mark Event Voltage.
- Due to possibility of slow port discharge and lack of clear definition in standard, timing could be interpreted as occurring when port enters Mark Event Voltage range.

New Mark Timing Solution

- TBD

New Turn On Delay Issue

- When Type 2 PDs is powered, it is powered up with Type 1 current and power limits.
- After power up, PSE transitions the power supply from Type 1 level to Type 2 level.
- The time when this occurs will depend on the classification type.
  - 2-Event classification will allow system to transition soon after power_on.
  - 1-Event + Layer 2 classification will take longer time period (1-2 minutes?) before the change is made.
- Finite time is required for PSE to make transition from low power to high power.
- PD must wait until PSE transition from low power to high power is complete before drawing higher current.
- This timing requirement is not currently specified in the standard.