PoE Plus
IEEE 802.3at
Classification Ad Hoc

Resolving Draft 1.0
Comments in L1 Bucket

Clay Stanford
Linear Technology
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Teleconference

Cl 33 SC 3.4.2 P 57 L 38 # 255

Stanford, Clay Linear Technology

Comment Type E *Comment Status* D *L1 adhoc*

Define Mark Event Voltage range. It will make text more clear.

Define Reset Voltage range. It will make text more clear.

Label Reset Threshold Vreset_th to be more consistant.

SuggestedRemedy

Table 33-11a

Item 2: Add "10" to max column.

Item 5: Change Symbol from Vreset to Vreset_th

Add new item 6, Classification Reset Voltage Vreset V 0(V) 2.8(V) See 33.3.4.2.1

Proposed Response *Response Status* O

see 256

Cl 33 SC 3.4.2.1 P 57 L 53 # 256

Stanford, Clay Linear Technology

Comment Type E *Comment Status* D *L1 adhoc*

Text will be more clear if we use Vmark range.

SuggestedRemedy

Line 53 IS:

When the voltage at the PI is between VMark min and VMark_th min, a Type 2 PD shall return a non-valid detection signature as defined in Table 33–9.

Line 53 SHOULD BE:
When the voltage at the PI is IN THE RANGE OF Vmark, a Type 2 PD shall return a non-valid detection signature as defined in Table 33–9.

Proposed Response *Response Status* O

see 255

Table 33–11a—2-Event Physical Layer classification electrical requirements

Item	Parameter	Symbol	Units	Min	Max	Additional Information
1	Class Event Voltage	V_{Class}	V	14.5	20.5	
2	Mark Event Voltage	V_{Mark}	V	6.9		
3	Mark Event Current	I_{Mark}	mA	0.25	2	See 33.3.4.2.1
4	Mark Event Threshold	V_{Mark_th}	V	10	14.5	See 33.3.4.2.1
5	Classification Reset Threshold	V_{Reset}	V	2.8	6.9	See 33.3.4.2.2

10V

Ad hoc group accepts comments 255 and 256 without opposition, however see comment below.

Vreset_th

6 | Classification Reset Voltage | Vreset| V | 0 | 2.8 | See 33.3.4.2.1

Add this new entry

It was commented that standard needs margin between PSE and PD voltage ranges by making PSE <= while PD is just <. This desire is covered in PD state machine where state transitions occur when Vport<mark_th, for example.

Cl 33 SC 2.7.2a P 38 L 40 # 83

Darshan, Yair — Microsemi Corporation

Comment Type TR Comment Status D L1 adhoc

Draft 1.0:
If after Iclass_lim event the PSE classify the PD as class 4, why we need to be in Reset range?
It looks that the text "Subsequent to such classification, the PSE shall ensure that the voltage at the PI enters the VReset range for at least TReset min as defined in Table 33-4a prior to powering the port." is not required.

SuggestedRemedy

Option a:
Classification ad hoc to explain why we need it.
If we don't need it, to delete it.

Option b:
Change the text to read:
"If PSE decides not to complete two event classification due to any reason, or decides to ignor classification results, the PSE shall ensure that the voltage at the PI enters the VReset range for at least TReset min as defined in Table 33-4a prior to powering the port."

Proposed Response Response Status O

←Accept in principle
OBE
See 149

Cl 33 SC 2.7.2a P 38 L 35 # 130

Schindler, Fred — Cisco Systems

Comment Type ER Comment Status D L1 adhoc

The text:
"… transition to the POWER_ON state without allowing the voltage at the PI to go below Vmark." Conflicts with text at L40: "… shall ensure the PI enters the Vreset range…" because Vmark > Vreset.

SuggestedRemedy

Have the L1 ad hoc provide text to correct this section.

Proposed Response Response Status O

defer to L1

←Accept in principle
OBE
See 149

If any measured IClass is equal to or greater than IClass_LIM min as defined in Table 33–4a, the PSE shall classify the PD as Class 04. If any measured IMark is greater than or equal to IMark_LIM min as defined in Table 33–4a, the PSE shall classify the PD as Class 0. **Subsequent to such classification, the PSE shall ensure that the voltage at the PI enters the VReset range for at least TReset min as definied in Table 33–4a prior to powering the port.**

Cl 33 SC 33.2.7.2a P 38 L 41 # 149

Beia, Christian — STMicroelectronics

Comment Type TR Comment Status A

If the measured Iclass is greater than Iclass_lim, the assigned class is Class4. There is no reason to reset the voltage at the PI in this case. Whithout this sentence, if the 2-event classification succeded, the PD will work correctly as class 4.
With a reset instead, the PD will work as a Type1 PD, wasting a lot of the allocated by the PSE.

SuggestedRemedy

Remove the sentence:
Subsequent to such classification, the PSE shall ensure that
the voltage at the PI enters the VReset range for at least TReset min as definied in Table 33–4a prior to powering the port.

Response Response Status C

ACCEPT.

Cl 33 SC 2.7.2a P 37 L 52 # 129

Schindler, Fred — Cisco Systems

Comment Type TR *Comment Status* A *L1 adhoc*

The same settling requirements for Type-1 classification should be imposed on Type-2 first class, classification. A Type 1 PD requires 5 ms to provide a valid class current (table 33-12, item 9). This comment also applies to p38 L24.

SuggestedRemedy

Have the L1 ad hoc review and correct this section.

Response *Response Status* C

ACCEPT IN PRINCIPLE.

The editor to apply the same transient settling timing to both 1-event and 2-event classifications. Page 37, line 43.

Comment 245 was accepted and suggested aligning Type 1 and Type 2 class timing. However, editor instructions do not this state explicitly. Ad hoc suggests Table 33-4a, entry 10 minimum time changed from 10ms to 6ms.

Comment 129 suggests 1-Event and 2-Event PSEs should have same time measurement delay requirement. Ad hoc agrees.
Modify comment 243: Accept in principle, but change wording p37L43:
IS: Measurement to be taken after 6ms to ignore initial transients.
SHOULD BE: Measurement to be taken after Tpdc to ignore initial transients.
ADD p37L54: Measurement to be taken after Tcle1 to ignore initial transients.
ADD p38L28: Measurement to be taken after Tcle2 to ignore initial transients.

Cl 33 SC 2.8 P 41 L 38 # 245

Stanford, Clay — Linear Technology

Comment Type T *Comment Status* A

When the 2-event classification was created, it was desired to perform it quickly so the PSE miniumum timing was reduced from 10ms to 6ms. (The PD must be stable within 5ms.) There now is a discrepancey beteeen 1-event and 2-event classification in this minimum pulse period. It would be best to align the two timing numbers.

Also, Table 33-5 entry would make more sense moved to table 33-4a

SuggestedRemedy

IS:
Table 33-5, item 20
10mS minimum.

SHOULD BE:
6ms minimum.

Move entire line over to Table 33-4a.

Response *Response Status* C

ACCEPT IN PRINCIPLE.

Change title of moved line from "Classification timing" to "1-Event class timing"

add a new column titled "1-Event/2-Event"
1a = 1&2 event
1b = 1&2 event
2a - 9 = 2 event
item 10 (the new item) = 1 event

Cl 33 SC 3.4.2 P 57 L 50 # 111

Darshan, Yair Microsemi Corporation

Comment Type T *Comment Status* D *L1 adhoc*

Draft 1.0:
PD don't have to present class 4 for infinite classification attempts.
Id adds thermal burden and costs.
In any case if system has problems it may initiate consecutive startups every Ted which is defined in Table 33-5 item 21.

SuggestedRemedy

To be added after line 50.
"PD may revert to IDLE state if PSE initiate more then 3 consecutive classification attempts within less then Ted as specified in Table 33-5."

Proposed Response *Response Status* O

defer to L1

Sentence in Question: A Type 2 PD shall return a Class 4 signature irrespective of the number of classification voltage probes performed by a PSE.

Ad hoc suggests accept in principle.
Modify sentence P57,L50:
IS: A Type 2 PD shall return a Class 4 signature irrespective of the number of classification voltage probes performed by a PSE.
SHOULD BE: A Type 2 PD shall return a Class 4 signature FOR at LEAST THE FIRST 4 voltage probes performed by the PSE.

Cl 33 SC 2.7.2a P 38 L 40 # 102

Darshan, Yair Microsemi Corporation

Comment Type TR *Comment Status* D *L1 adhoc*

Draft 1.0:

When PSE classify the PD after Icllas_LIM event it should get to Vreset for Treset prior to power the port.

In order to achieve this objective PD should consume some minimum current to allow PSE to reduce its port voltage due the capacitors in the channel.

SuggestedRemedy

The classification ad hoc to adress this issue if it is possible to implement i.e. to have I>>0 at 2.8V to 6.9 Volt range for Treset.

Proposed Response *Response Status* O

defer to L1

Accept in principle.

Add the following at p58L13

The PD shall draw 0.25 mA minimum until the PD transitions from the Mark state to the Reset state.

We need to extend PSE Treset to insure port gets discharged.

dt = C dv/I = .7uf * 4.2V/.25mA = 12ms

Modify comment 267 (p39L30) from 5ms to 15ms.

IS THIS OK WITH AD HOC PARTICIPATES?

Cl 33 SC 2.7 P 36 L 27 # 127

Schindler, Fred Cisco Systems

Comment Type TR *Comment Status* D *L1 adhoc*

The text:
"If a PSE successfully completes detection of a PD, but the PSE fails to complete classification of a PD, then a Type 1 PSE shall assign the PD to Class 0 and a Type 2 PSE shall assign the PD to class 4." imposes an unnecessary design requirement. This text also enables dump-Type 2 PDs that do not support DLL classification.

A system that does not provide a proper class is:
a) Experiencing a temporary fault that will rectify itself.
OR
b) Noncompliant.

A compliant Type-2 PD has not achieved mutual identification and will remain in type-1 power mode. Therefore, requiring class-4 power serves no legitimate purpose.

A PSE that classifies a PD and gets an invalid results is not probable because this occurs only when class current exceeds 51 mA.

SuggestedRemedy

Require PSEs that performs classification, to either repeat the detection and classification steps, or repeat the classification step, until legal responses are achieved.

Proposed Response *Response Status* O

defer to L1

Will require full committee discussion.

New Mark Timing Issue

- PSE Mark Event timing
  Table 33-4a, item 4
  (D1.0, page 39, line 19)
- Though hardware as spec'ed will interoperate, port loading during event will effect observable timing behavior.
- Timing start and stop points are not clearly defined in standard.
- Due to lack of clear definition in standard, misinterpretation of timing could occur.
- Intent was for timing event to commence when PSE changes from Class mode to Mark mode.
- Intent was for timing event to end when PSE changes from Mark mode to Class mode.

New Mark Timing Solution

33.2.7.2a P38L21 TEXT IS:

The Type 2 PSE shall then provide to the PI VMark as defined in Table 33–4a. The timing specification shall be as defined by TME1 in Table 33–4a. This first VMark provision is known as the first mark event.

The Type 2 PSE shall then provide to the PI the second class event, subject to the VClass and TCLE2 definitions in Table 33–4a. The PSE shall measure IClass and again classify the PD based on the observed current according to Table 33–4.

Following successful completion of the second class event, the PSE shall provide a second mark event subject to the VMark and TME2 definitions in Table 33–4a.

33.2.7.2a P38L21 TEXT SHOULD BE:

The Type 2 PSE shall then provide to the PI VMark as defined in Table 33–4a. This first VMark provision is known as the 1st mark event. The PI VMark requirement is to be met with load currents in the range of 0.25 to 2mA. In a properly operating PoE system, the port may or may not discharge to the VMark range due to the combination of channel capacitance and PD current loading. This is normal and acceptable PoE system operation. For compliance testing, it is necessary to discharge the port in order to observe the VMark voltage. Discharge can be accomplished with a 2mA load for 3mS, after which VMark can be observed with minimum and maximum load current.

The first mark event timing specification shall be as defined by TME1 in Table 33–4a. The mark event commences when the PI voltage falls below VClass_min and ends when the PI voltage exceeds VClass_min.

New Mark Timing Solution Cont'

33.2.7.2a P38L30 TEXT IS:

Following successful completion of the second class event, the PSE shall provide a second mark event subject to the VMark and TME2 definitions in Table 33–4a.

33.2.7.2a P38L21 TEXT SHOULD BE:

Following successful completion of the second class event, the PSE shall provide a second mark event subject to the VMark and TME2 definitions in Table 33–4a. The mark event commences when the PI voltage falls below the VClass_min and ends when the PI voltage exceeds VClass_min. There is not a specified TME2_max, however per 33.2.8.13, if the PSE is to power a PD, it is required to do so within Tpon.

New Mark Timing Solution Cont'

Table 33–4a—Type 2 Physical Layer classification electrical requirements

Item	Parameter	Symbol	Units	Min	Max	Additional Information
1a	Class Event Voltage	V_{Class}	V	15.5	20.5	
1b	Class Event Current Limitation	I_{Class_LIM}	mA	51	100	
2a	Mark Event Voltage	V_{Mark}	V	7	10	0.25mA≤ILoad≤2mA See 33.2.7.2a
2b	Mark Event Current Limitation	I_{Mark_LIM}	mA	5	100	
3	1st Class Event Timing	T_{CLE1}	ms	6	30	
4	1st Mark Event Timing	T_{ME1}	ms	6	12	See 33.2.7.2a
5	2nd Class Event Timing	T_{CLE2}	ms	6	30	
6	2nd Mark Event Timing	T_{ME2}	ms	6		~~Time from end of detection until power on is limited by 33.2.8.13.~~
7	3rd Class Event Timing	T_{CLE3}	ms		30	
8	Classification Reset Voltage	V_{Reset}	V	0	2.8	
9	Classification Reset Timing	T_{Reset}	ms	TBD	TBD	

See 33.2.7.2a

New PD Class to Mark Current Issue

- The required current draw of the PD as it transitions from Class to Mark is not clearly defined.
- The PD must continue to draw current in order for the port to discharge.
- We will add text to clarify the operation in this range.

New PD Class to Mark Solution

P57L50 TEXT IS (with implementation of accepted and expected comments)

33.3.4.2.1 Mark Event behavior

When the voltage at the PI is within the range of VMark, a Type 2 PD shall return a non-valid detection signature as defined in Table 33–9.

A Type 2 PD must return a Class 4 signature when voltage at the PI is in the range of Vclass. A Type 2 PD must draw IMark when voltage at the PI is in the range of VMark.

A Type 2 PD shall not exceed the IMark current limits when voltage at the PI enters the VMark specification as defined in Table 33–11a.

P57L50 TEXT SHOULD BE(with implementation of accepted and expected comments)

33.3.4.2.1 Mark Event behavior

When the voltage at the PI is within the range of VMark, a Type 2 PD shall return a non-valid detection signature as defined in Table 33–9.

A Type 2 PD must return a Class 4 signature when voltage at the PI is in the range of Vclass. A Type 2 PD must draw IMark when voltage at the PI is in the range of VMark.

A Type 2 PD shall not exceed the IMark current limits when voltage at the PI enters the VMark specification as defined in Table 33–11a.

As the PD is changing from Class to Mark state, it shall transition from the Class 4 signature current to the Mark current. This transition shall occur in the range of Vmark_th. During this transition, the PD shall draw at least IMark_min current.

We don't need to address the transition from Mark to State because the PSE will drive the port high regardless of current.

New Turn On Delay Issue

- When a Type 2 PD is powered, it is powered up with Type 1 current and power limits.
- After power up, PSE transitions the power supply from Type 1 level to Type 2 level.
- The time when this occurs will depend on the classification type.
  - 2-Event classification will allow system to transition soon after power_on.
  - 1-Event + Layer 2 classification will take longer time period (1-2 minutes?) before the change is made.
- Finite time is required for PSE to make transition from low power to high power state.
- PD must wait until PSE transition from low power to high power is complete before drawing higher current.
- This timing requirement is not currently specified in the standard.
- We need to add a low-power to high-power transition delay in the PD section.