IEEE802.3poep Study Group

4P HP vs 2P HP
What is the best system decision

San Francisco July 2005

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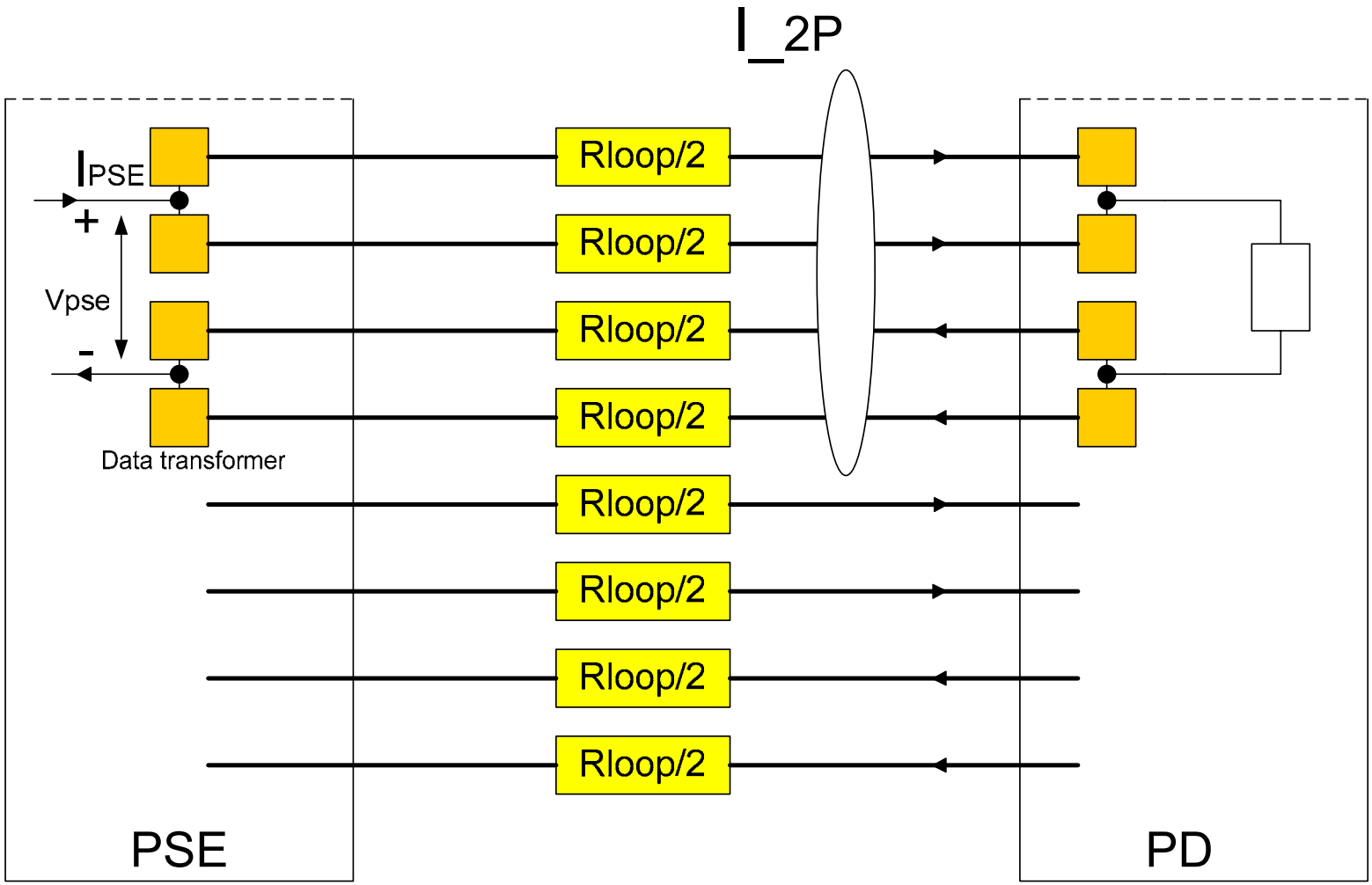
Main points of discussion

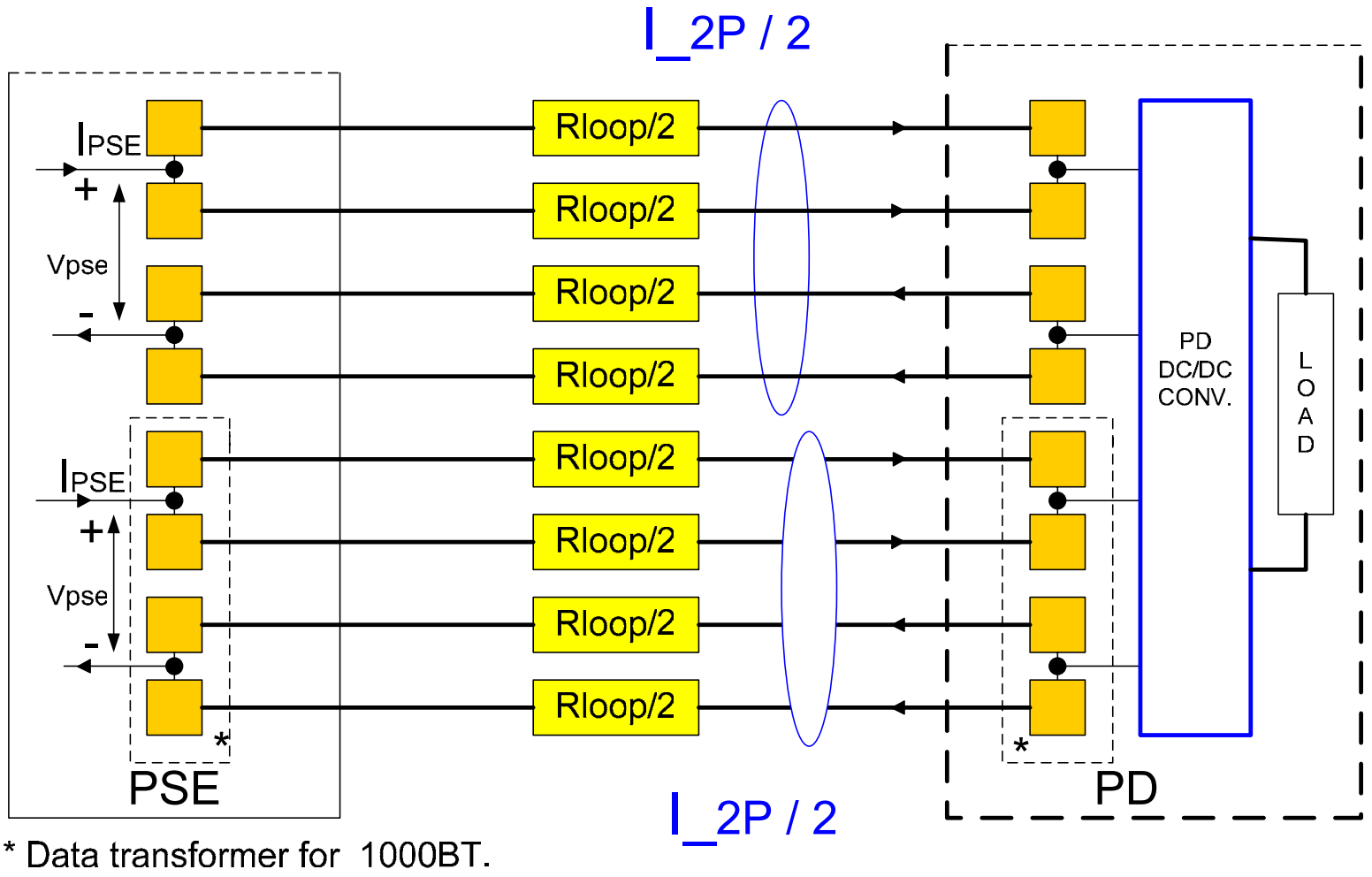
- Summary of inputs received from previous meetings

- Main challenges
  - Does 4P cost more than 2P
  - Is there a place for three standards?
    - Should 2P medium HP be addressed in the standard in addition to 4P high power and 2P IEEE802.3af

Power Feeding Methods Introduction – 2P

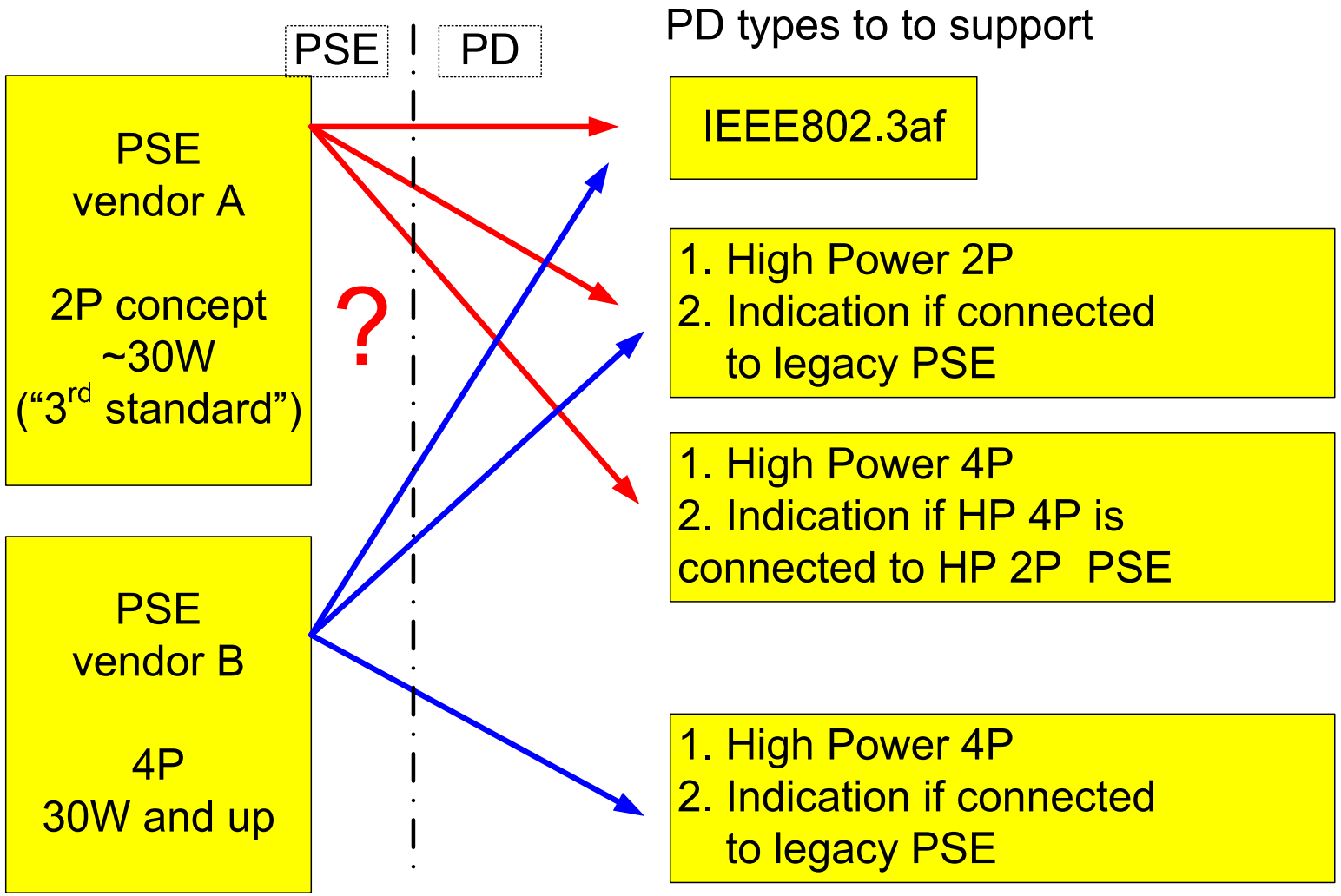


Power Feeding Methods Introduction – 4P

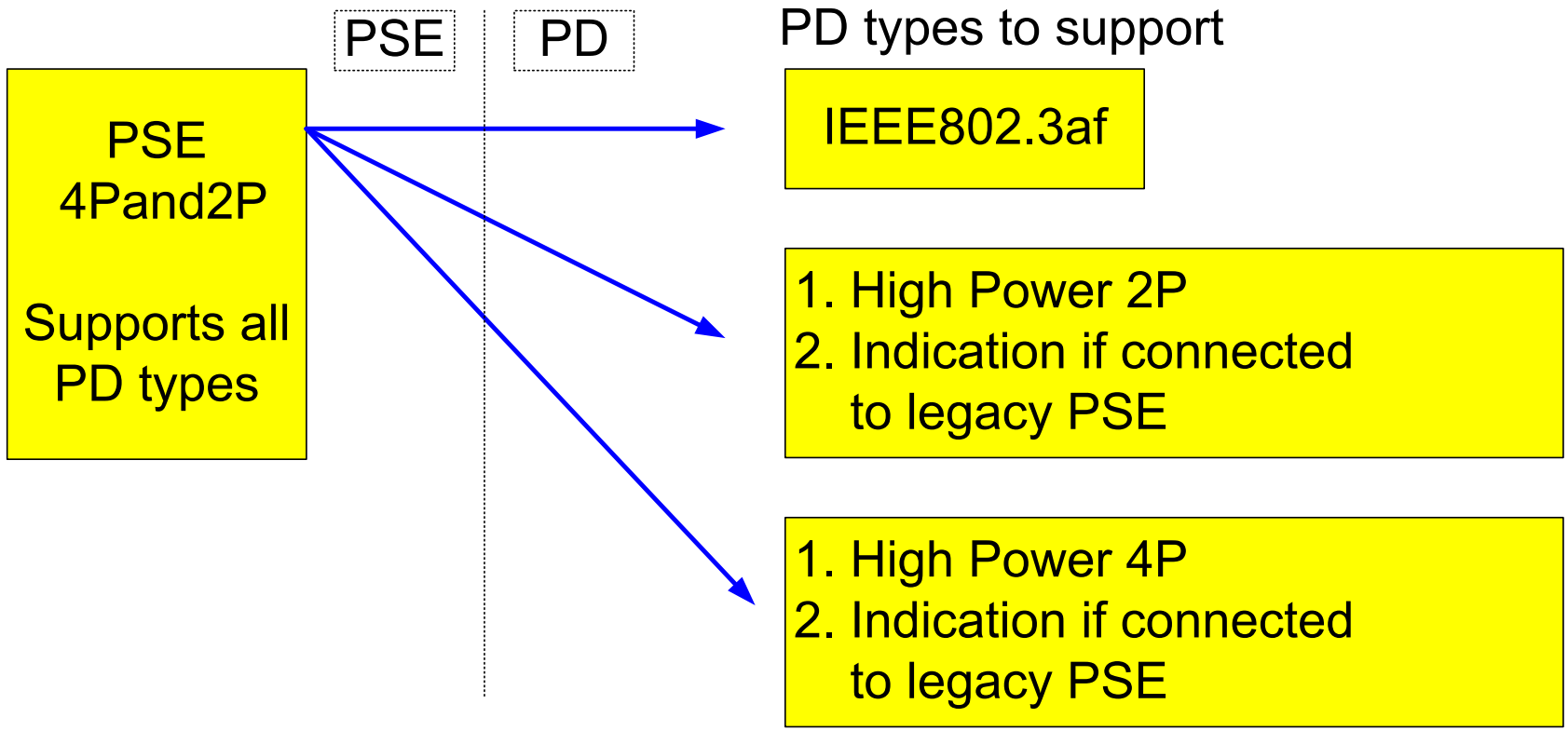


* Data transformer for 1000BT.

Power Feeding Methods Introduction - 2Por4P



Power Feeding Methods Introduction - 2Pand4P



Summary of inputs received in previous meetings

- May 2005, Clay Stanford/LT and others
  - 4P system is necessary solution due its ability to supply maximum power within practical limits as per our project objective.
- May 2005, Clay Stanford/LT, March 2005, Yair Dashan/PowerDsine,
  - Implementing 4P (with IEEE802.3af current levels) – the fastest way to get high power
- March 2005, Steve Ellsworth
  - The proposed 2P load current for POE Plus will have a significant effect on the interface transformers used in today's LAN interface.
- March 2005, Hank Hinrichs/Pulse
  - A more serious problem is the impact increasing PoE current has on the transformer's inductance.
- March 2005, Ron Nordin, Panduit
  - Recommendation to utilize all 4 pairs due to temperature rise and less power dissipation

Summary of inputs received in previous meetings
Open points for discussion

- Does 4P cost more than 2P
- Is there a place for three standards?
  - 2P, IEEE802.3af
  - 4P, IEEE802.3poep
  - 2P, IEEE802.3poep2
    - Should 2P medium HP be addressed in the standard in addition to 4P high power and 2P IEEE802.3af

Doe's really 4P cost more than 2P?

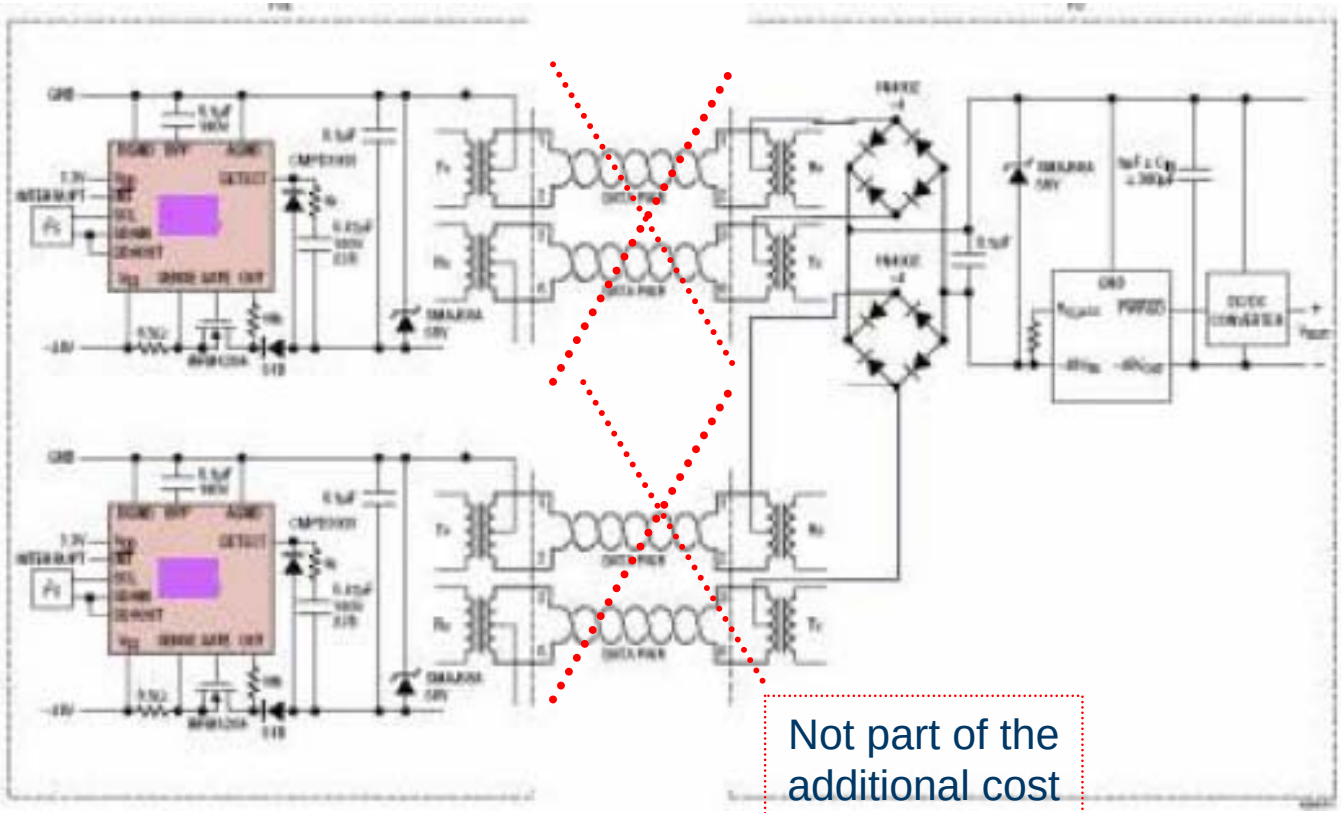
- Let’s address in short the following issues
  - Chip cost
  - PSE PS cost
  - Cables power dissipation
  - Chip power dissipation
  - Enhanced classification costs
  - Connectors reliability
  - Data transformer
    - Size
    - Current imbalance
    - RF performance
    - Temperature rise
  - Standard components vs custom components
  - Supporting objective 13
  - Supporting 4P$_{AND}$2P , 4P$_{OR}$2P

Does really 4P cost more than 2P?

- Part 1: Focusing on PSE
  - Chip level
  - System level

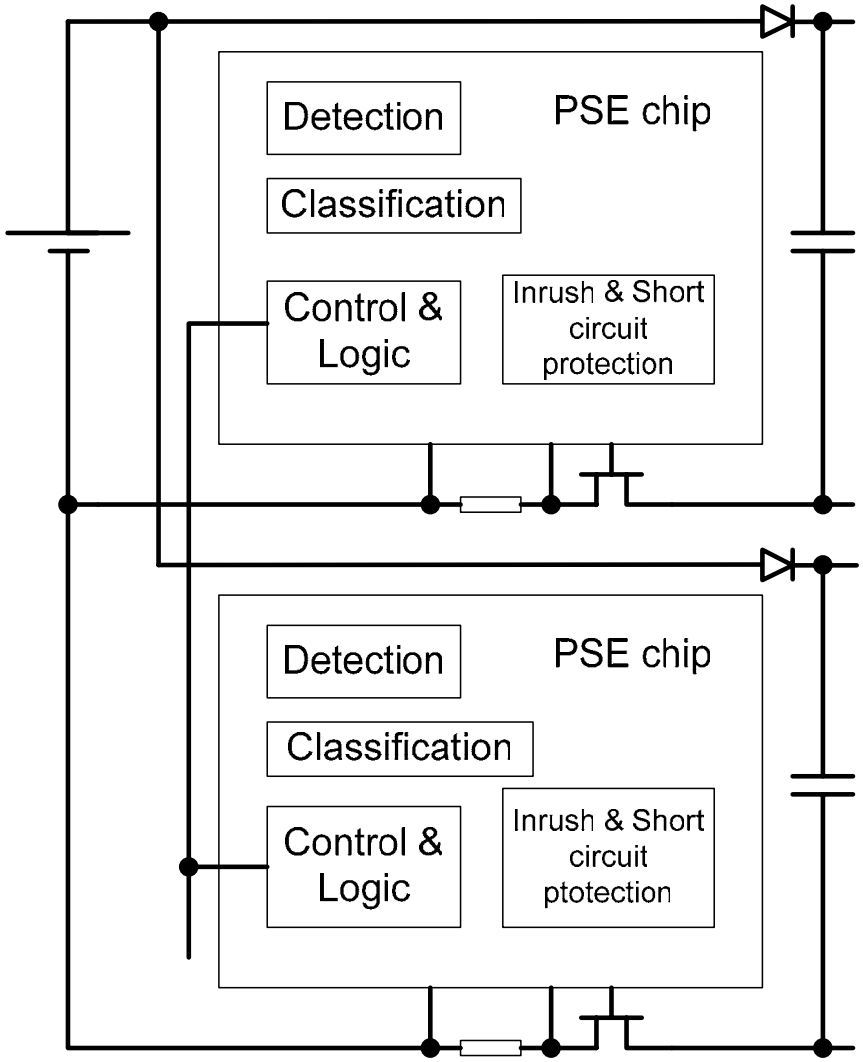
Doe's really 4P cost more than 2P?

- From previous meeting. This is expensive solution.
- Not fits for cost analysis.



Taken from May 2005, Clay Stanford presentation

Does really 4P cost more than 2P?



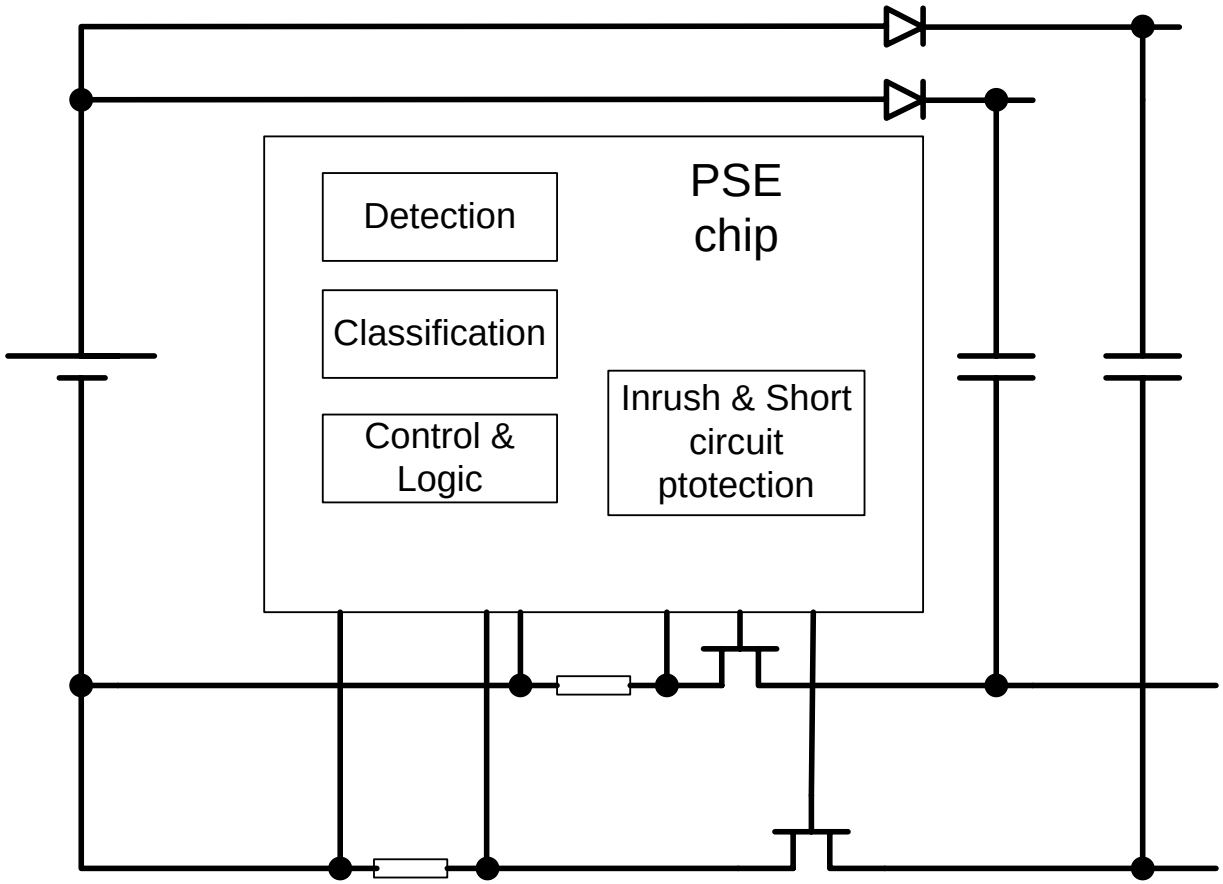
Simplified version of the previous drawing.

Not fit for cost analysis

The following 4P concept is expensive…however there is a much lower cost option.

Does really 4P cost more than 2P?

- How about using single chip instead of two old chips?



Does really 4P cost more than 2P?

- All functions such detection, classification control and logic are similar in both concepts.
  - Additional costs and complexity 4Pand2P and 4Por2P.
- Additional external components in 4P compared to 2P
  - Additional sense resistor, output capacitor and optional diode.
  - Additional external Mosfet (smaller than required in 2P).
- Total additional cost for chip level: 20% max more compared to 2P.

Does really 4P cost more than 2P?

- Chip power dissipation
  - 4P can shorten extended classification time by easily coding the two ports classification results resulting with lower chip power dissipation and cost as demonstrated in March 2005.

Does really 4P cost more than 2P?

- Enhanced classification costs
  - 4P can reduce logic and control costs of extended classification concepts by easily coding the two ports classification results.

Does really 4P cost more than 2P?

- PSE Power Supply cost
- Any power loss on cables due to higher currents will add to PSE PS requirements hence add cost to the system
  - 9% more at 30W for 2P compared to 4P.

Does really 4P cost more than 2P?

- Cables power dissipation in 2P
  - Increased temperature rise in 2P
  - Higher sensitivity to RF performance
  - Limited available max power due to larger design margins required
  - Risks for supporting 10G?
- All results with higher risks and may results with reduced performance and reliability.
- 4P has significantly lower risks at the above issues

Does really 4P cost more than 2P?

- Connectors reliability in 2P
  - Connector contacts resistance is function of current and voltage combination.
  - Higher current results with reduced reliability
  - Need to investigated more by the ad-hoc team

Connectors reliability In 4P:

Mature environment. Significantly lower risks.

Does really 4P cost more than 2P?

- PHY resiliency to dv/dt In 2P:
  - Higher current is 2P results with higher risks such high dv/dt due to high di/dt during PD hard disconnection which may damage PHY

In 4P:

- Mature environment. Significantly lower risks.

Does really 4P cost more than 2P?

- Data transformer current imbalance is significant problem in 2P
  - It can be handled partly by increasing core size however RF parameters integrity are at risk
  - Temperature rise still need to be solved
  - It increases size of solution and will exclude applications that requires dense packaging.
  - It will create a custom solution without utilizing a standard solution such as in 4P hence lower quantities and higher costs
  - Current imbalanced can also handled by active current balancing which will add 30% more cost to the PD chip. Temperature rise still unsolved.

Does really 4P cost more than 2P?

- Supporting objective 13
  - Need to support overload for reduced class per port
  - Add more cost to 2P
- Simple with 4P
  - No need for overload per class per port

Does really 4P cost more than 2P?

- Supporting 4P AND 2P
- Need to support 4P HP and 2P Medium power enhanced classification
  - More logic & control, Increased cost
- Need to support overload per port per class
  - More logic & control, Increased cost

Does really 4P cost more than 2P?

- Supporting 4POR2P
  - Vendor A: Will use HP 2P (TBD standard)
  - Vendor B: Will use HP 4P (IEEE802.3poep)
- They need to support:
  - IEEE802.3af PD
  - IEEE802.3poep 4P PD
  - TBD standard 2P HP PD
- Two solution to three problems vs the IEEE requirement of single solution to a single problem? Is this still a standard?
  - Increased cost for each solution
  - Complex interoperability issues to be addressed
  - dilution of all standards, causing lower quantities and increased solution price, as well as confusion in the market and slower adaptation curves for BOTH.

PSE: Chip level

#	Parameter	2P	4P
1	Additional external components (including Mosfet) in 4P	1	~1.2
2	Current limit per port per class to support 2P	>1.03-1.05	1
3	Additional cost in enhanced classification due to thermal issues (due too less options for coding)	1+k1	
4	**Total**	**1+0.03+k1**	**1.2**

PSE chip level: 4P may cost a bit more than 2P

All numbers are ratio representation

PSE: System level

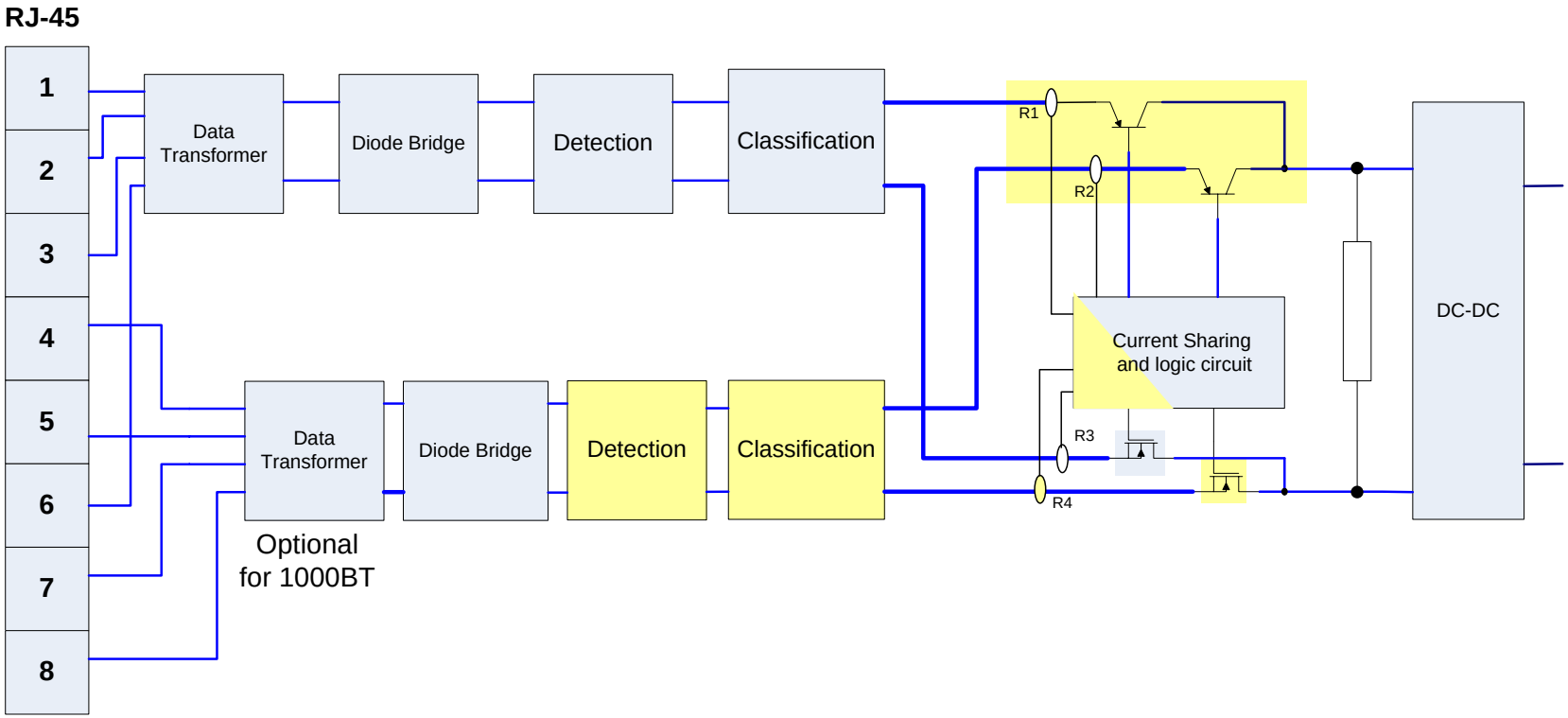
#	Parameter	2P	4P
4	PSE chip additional costs	**1+0.03+k1**	**1.2**
5	Additional power supply cost due to power loss on cables in 2P.	1.09	1
6	Additional cost per higher power dissipation in 2P	1+k2	1
7	Additional long term reliability cost on connectors due to higher current in 2P	1+k3	1
8	Additional cost of increased temperature rise in data transformer in 2P	1+k4	1
9	Additional cost of increased data transformer size	1+k5	
10	Additional cost of Risks and other unknowns	1+k6	1
	Total PSE system cost	**1.12+k1..k6**	1.2
Total for PSE: 2P cost more than 4P at system level			

All numbers are ratio representation

Doe's really 4P cost more than 2P?

- Part 2: Focusing on PD
  - Chip level
  - System level

PD – Low cost 4P implementation -1



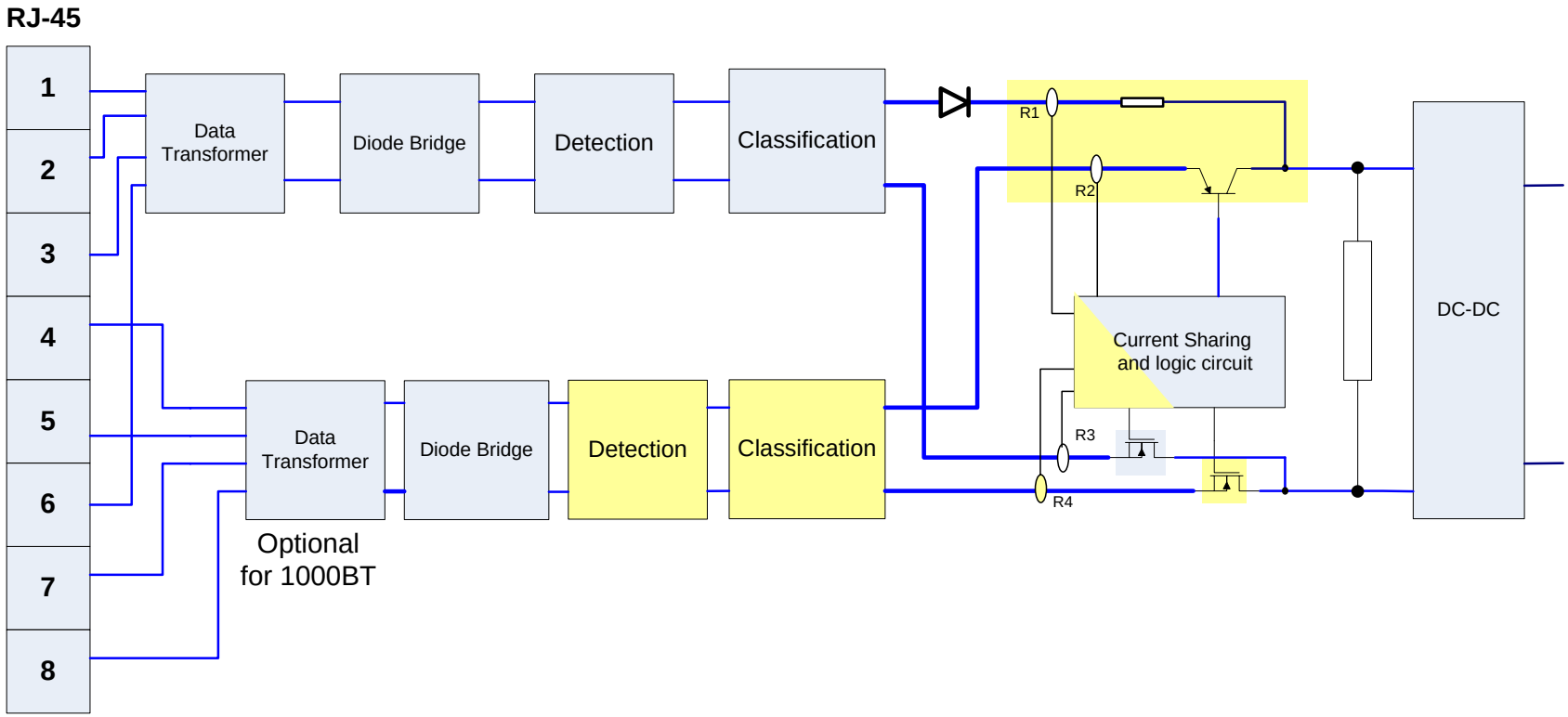
1. Low cost 4P solution for 10/100/1000BT including:

1.1 current sharing on all power rails

1.2 Enhanced classification flexibility compared to 2P

1.3 Current sharing should be in PD and not in PSE due too thermal considerations in PSE and better cost optimization in PD

PD – Lower cost 4P implementation - 2

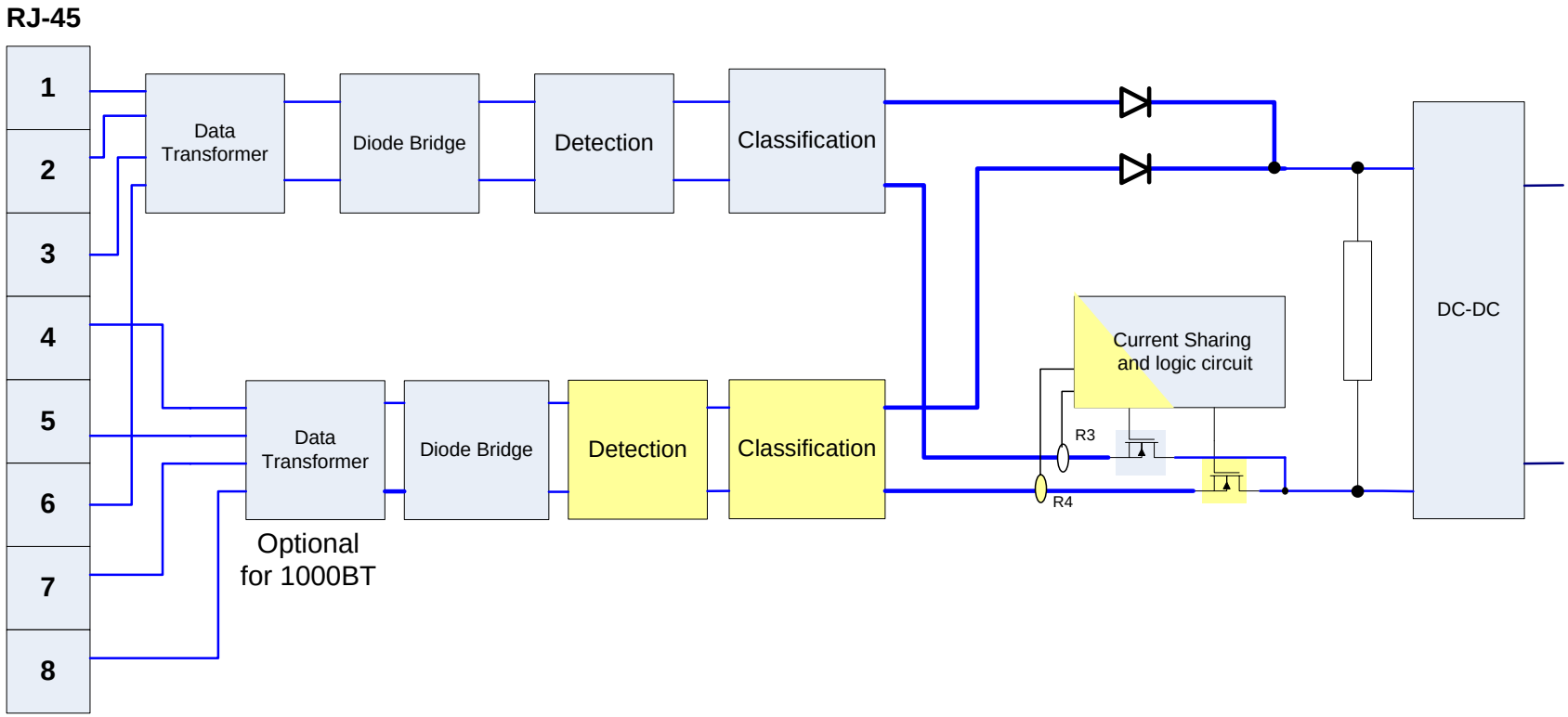


1. Low cost 4P solution for 10/100/1000BT including:

1.1 current sharing on all power rails, reduced cost on positive rail

1.2 Enhanced classification flexibility compared to 2P

PD – Lower cost 4P implementation - 3

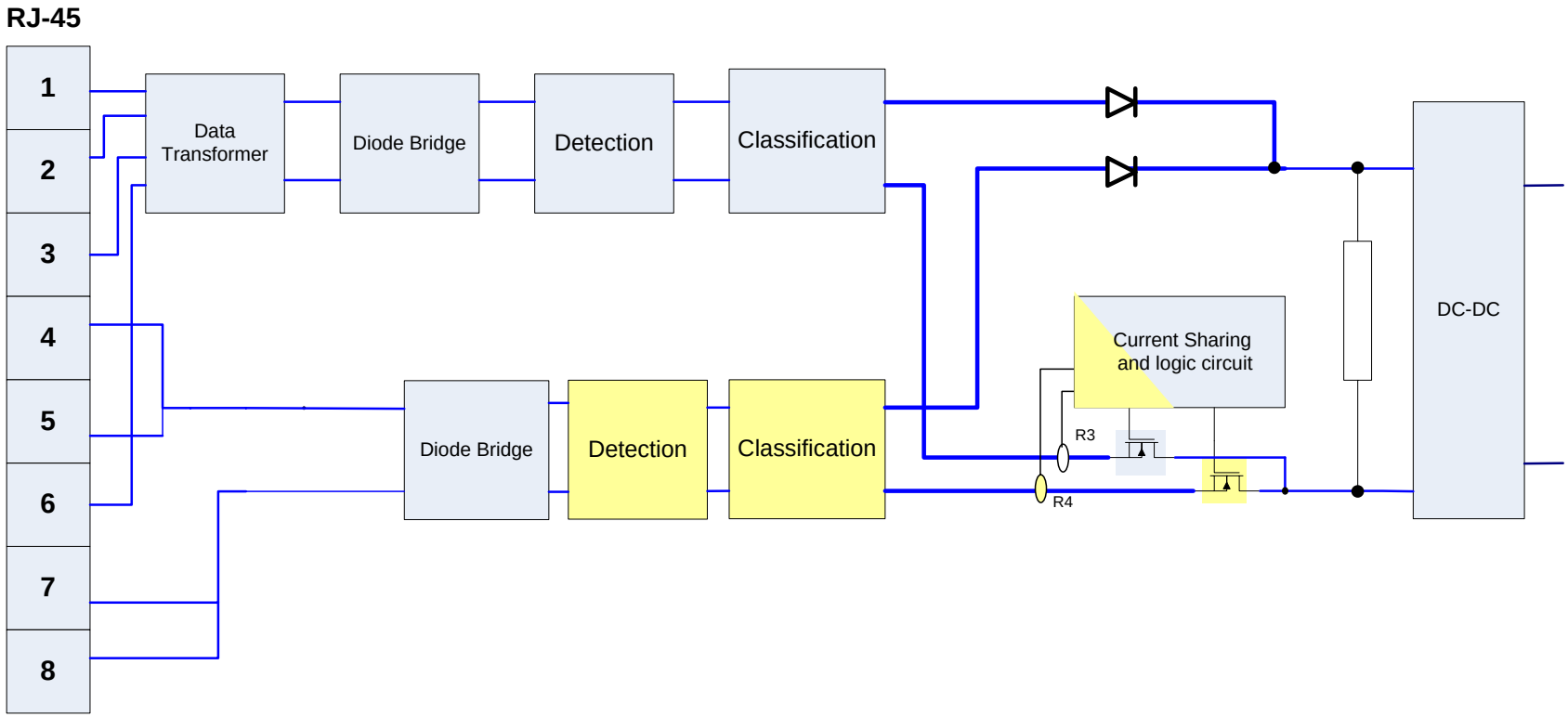


1. Low cost 4P solution for 10/100 including:

1.1 current sharing on negative rails only.

1.2 Enhanced classification flexibility compared to 2P

PD – Lowest cost 4P implementation - 4

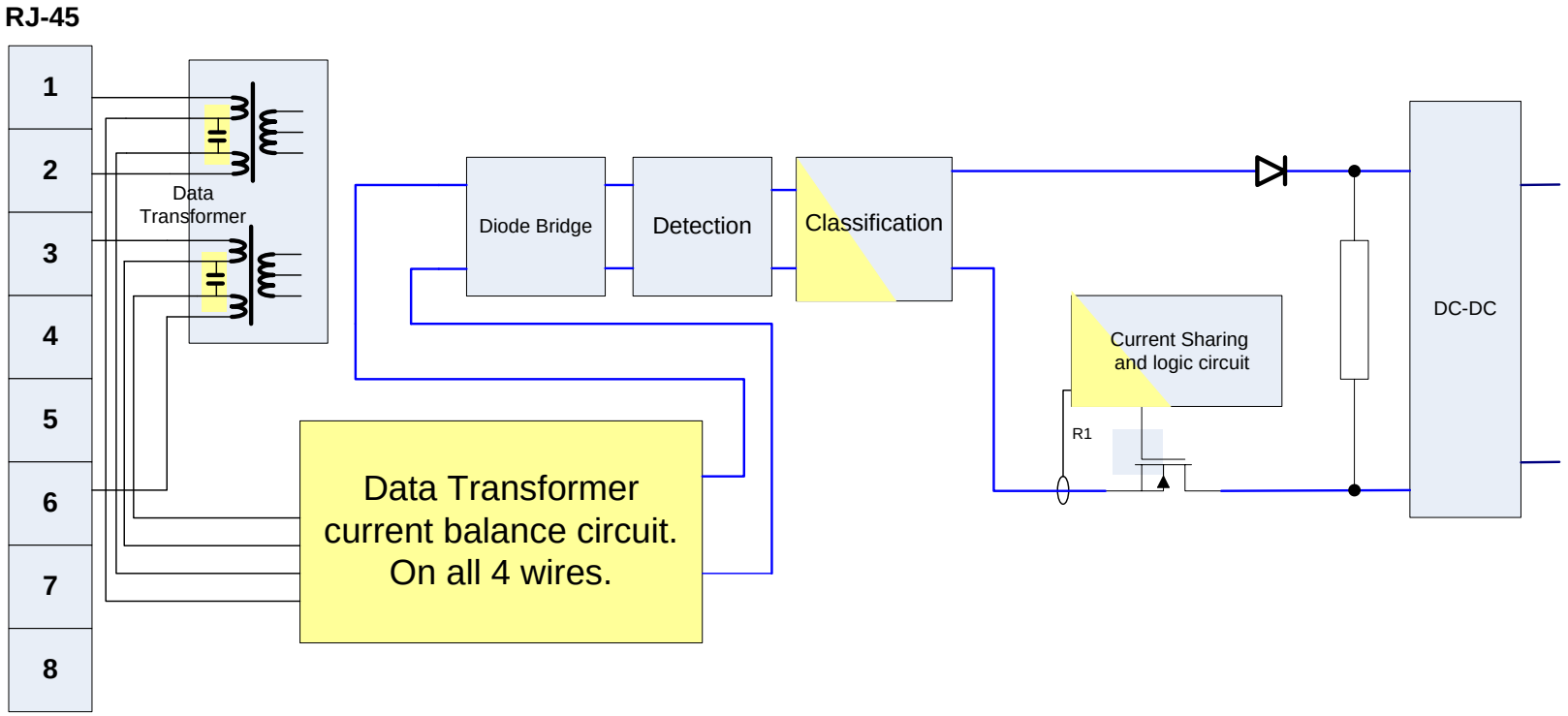


1. Tested low cost 4P solution for 10/100 including:

1.1 Current sharing on negative rails only. The Mosfet on the data pair may be smaller.

1.2 Enhanced classification flexibility compared to 2P

PD –2P HP implementation



1. 2P HP concept with Iport>350-400mA

1.1 Assuming that we can not increase data transformer size and solving RF and temperature issues due to the change

1.2 Additional circuitry for enhanced classification

1.3 Additional circuitry for handling high current/heat

1.4 Current balancing should be in PD and not in PSE due too thermal considerations in PSE and better cost optimization in PD

PD: Chip level

#	Parameter	2P	4P
1	Additional components in 4P- Detection	1	~1.005
2	Additional components in 4P- Classification	1	~1.02
3	Additional cost in 2P for enhanced classification (compared to 4P in terms of coding the class data and reducing power dissipation See annex A for example)	1+k1	1
4	Additional components in 4P- Isolating switch and current limit	1	~1.06
5	Additional components in 4P- current sharing for combining power from both data and non-data pairs for using single DC/DC converter	1	~1.3
6	Additional cost in 4P for handling UVLO timing between channels	1	1.03
7	Additional cost to balance data transformer current in 2P (700mA) assuming not increasing magnetic core and volume	+1.3	1
	Handling the effect of current balance components on RF performance	1+k2	1
8	DC/DC converter	1	1
9	**Total**	**1.3+k1+k2**	**1.415**
PD chip level: 4P cost about the same as 2P.			

PD: System level

#	Parameter	2P	4P
10	PD chip additional costs	**1.3+k1+k2**	**1.415**
11	Additional cost per higher power dissipation in 2P	1+k1	1
12	Additional long term reliability cost on connectors due to higher current in 2P	1+k2	1
13	Additional cost of increased temperature rise in data transformer in 2P	1+k3	1
	Total	1.3+k1+k2+k3+k4+k5	1.415
	TOTAL for PD: 2P cost more than 4P at system level		

Doe's really 4P cost more than 2P?

- 4P and 2P cost about the same.
- 4P cost less then 2P in $/W (from Economical Feasibility /CFI)
  - Absolute cost *is not the key* parameter that will make a difference in future comparison table
- 4P vs 2P should be evaluated for:
  - Features
  - Reliability
  - Risks
  - Overall system power efficiency (watts)
  - Sensitivity of RF performance to high currents/power dissipation/ temperature variations (1G, 10G ?)
  - System design flexibility
  - Simple standard (4P) vs Complex one (2P, 2Por4P and 2Pand4P)
  - Custom (2P) vs Standard (4P) components
  - Future market needs
  - Etc.

Summary

- 4P is required in the future standard
- 2P is the IEEE802.3af and is already there.
  - No need for 3rd 2P standard.
- 4P has the shortest time table
- 4Pand2P and 4Por2P
  - Will cost more then 4P alone or 2P alone.
  - Complex and risky then 4P alone or 2P alone.
- 4P-2P cost difference is negligible
  - From system point of view, 4P cost less than 2P
- 4Por2P is too complex. Multiple solutions to multiple problems. Major interoperability issues. Increased cost for all..
- 4P wins the “best standard” category.

4P

2P

Cost

System

2P

4P

Performance

2P

4P

Best Standard

Annex A – Example for how 4P can simplify enhanced classification by coding both channels

4P concept: Getting high resolution classification

- Classes 1-4 generates:
  - 20 HP levels
  - 5 AF levels
- If ch-1 and ch-2 are designated to the pair type (data or spare or pin numbers).
- More levels can be generate if more classes added.

Using enhanced classification based on time as presented in May 2005 can be enhanced by using both channels for coding

Meaning	Reading	ch-2 Pins 4,5,7,8	ch-1 Pins 1,2,3,6
AF, NO CLASS, 15.4W	**AF CLASS 0**	**0**	**0**
coding of different combinations of HP	HP CLASS 1	1	0
coding of different combinations of HP	HP CLASS 2	2	0
coding of different combinations of HP	HP CLASS 3	3	0
coding of different combinations of HP	HP CLASS 4	4	0
coding of different combinations of HP	HP CLASS 1	0	1
AF, CLASS 1, 4W	**AF CLASS 1**	**1**	**1**
coding of different combinations of HP	HP CLASS 5	2	1
coding of different combinations of HP	HP CLASS 6	3	1
coding of different combinations of HP	HP CLASS 7	4	1
coding of different combinations of HP	HP CLASS 2	0	2
coding of different combinations of HP	HP CLASS 5	1	2
AF, CLASS 2, 7W	**AF CLASS 2**	**2**	**2**
coding of different combinations of HP	HP CLASS 8	3	2
coding of different combinations of HP	HP CLASS 9	4	2
coding of different combinations of HP	HP CLASS 3	0	3
coding of different combinations of HP	HP CLASS 6	1	3
coding of different combinations of HP	HP CLASS 8	2	3
AF, CLASS 3, 15.4W	**AF CLASS 3**	**3**	**3**
coding of different combinations of HP	HP CLASS 10	4	3
coding of different combinations of HP	HP CLASS 4	0	4
coding of different combinations of HP	HP CLASS 7	1	4
coding of different combinations of HP	HP CLASS 9	2	4
coding of different combinations of HP	HP CLASS 10	3	4
AF, CLASS 4, Reserved or HP	**AF/HP CLASS 4**	**4**	**4**