

PoE+

Cost Effective Detection and Classification

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Motivation

- Extremely low implementation cost in PoE+ PD
- PoE+ PSE provides all signaling necessary for plus-PD to classify itself; plus-PD does not need independent notion of time or absolute voltage
- Limited increases in timing and voltage accuracy
- Accuracy improvements are placed in the plus-PSE, where they are most cost effective
- Robust interoperability with 802.3af equipment
- Plus-PD will know by design whether an af-PSE can provide adequate power

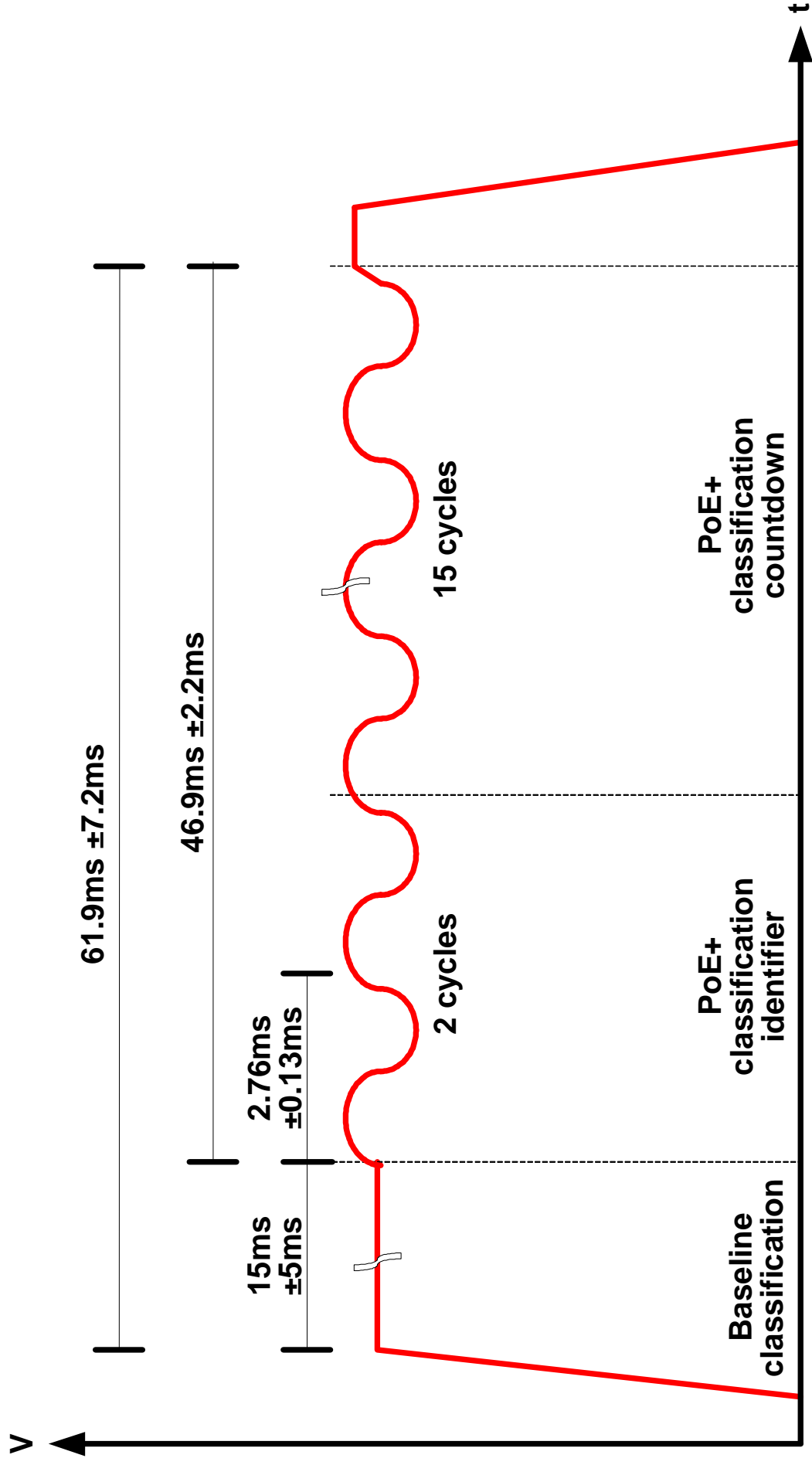
PoE+ Classification IS Detection

- PoE+ has meaning by virtue of its higher power delivery
 - Higher power needs can be communicated through classification
- End users have expressed desire for more precise classification
 - Proposed classification scheme also includes finer classification granularity
- Thus, the act of responding to a PoE+ PSE's classification request simultaneously identifies the PD as a 'plus-device' and describes its specific power requirement

Proposed PoE+ Classification

- Increase DC accuracy of Vclass: $18V \pm 1.2V$ (7%)
- Short period of standard classification time
- Followed by overlaying of a series of sinusoidal or trapezoidal waveforms on Vclass
 - Low enough freq. to meet EMI and data coherence needs: 400Hz $\pm 20\text{Hz}$ (5%)
 - Low enough amp. to meet 802.3af Vclass specification: 2.15Vpp $\pm 0.15V$ (7%)
- Plus-PD will use the AC signal as a clock to **early-terminate** its Iclass
 - indicates its power requirement
 - implicitly identifies itself as a PoE+ powered device

PoE+ Classification Details



PoE+ Classification Details

- Initial 15ms of Vclass establish the 'baseline' classification, i.e. class 0, 1, 2, or 3
- Two cycle signal indicates to PD the presence of a plus-PSE – a 'PoE+ Classification Identifier'
- Each baseline class is subdivided into 15 power levels by countdown ticks 0 through 14
- Each cycle that PD maintains Iclass indicates to the PSE a successively lower power level
 - e.g., for maximum power, PD will remove Iclass after seeing 2-cycle detection and countdown tick 0
 - If PD does not turn off during this time, it does not classify itself as a plus-PD, and is so baseline classified under the 802.3af definitions

PoE+ Classification Details

- Baseline Classes for plus-PDs:

Class	Iclassmin (mA)	Iclassmax (mA)	Pmaxlo (W)	Pmaxhi (W)
0	2	4	12.95	55.95
1	9	12	3.84	6.49
2	17	20	6.49	12.95
3	26	30	12.95	27.95
4	36	44	N/A	N/A

- Pmaxlo corresponds to Pmaxhi for af-PDs
- Need to have a measurable Iclassmin for class 0 (how can you tell when 0mA is 'turned off?')

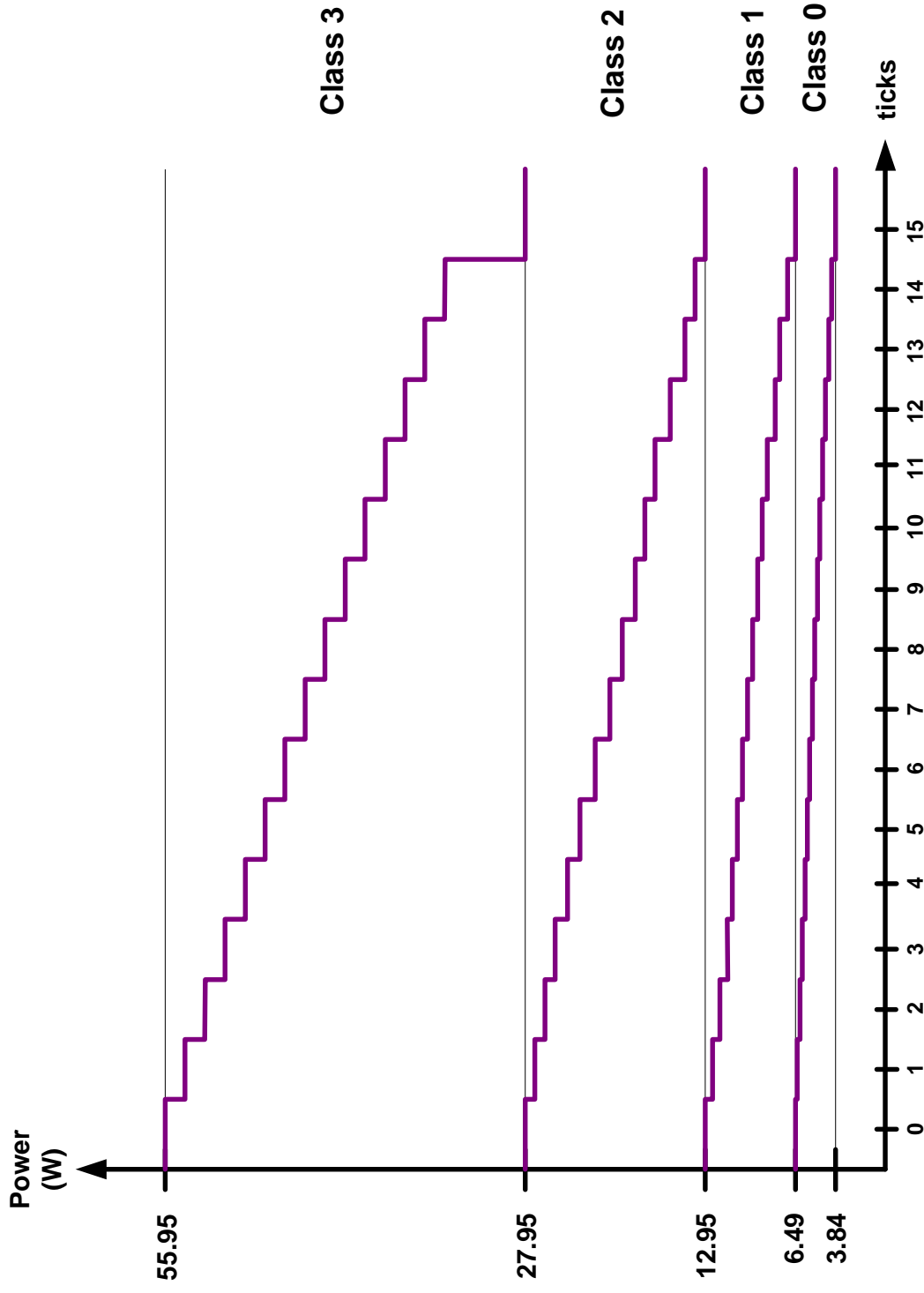
PoE+ Classification Details

- Class steps for plus-PDs:

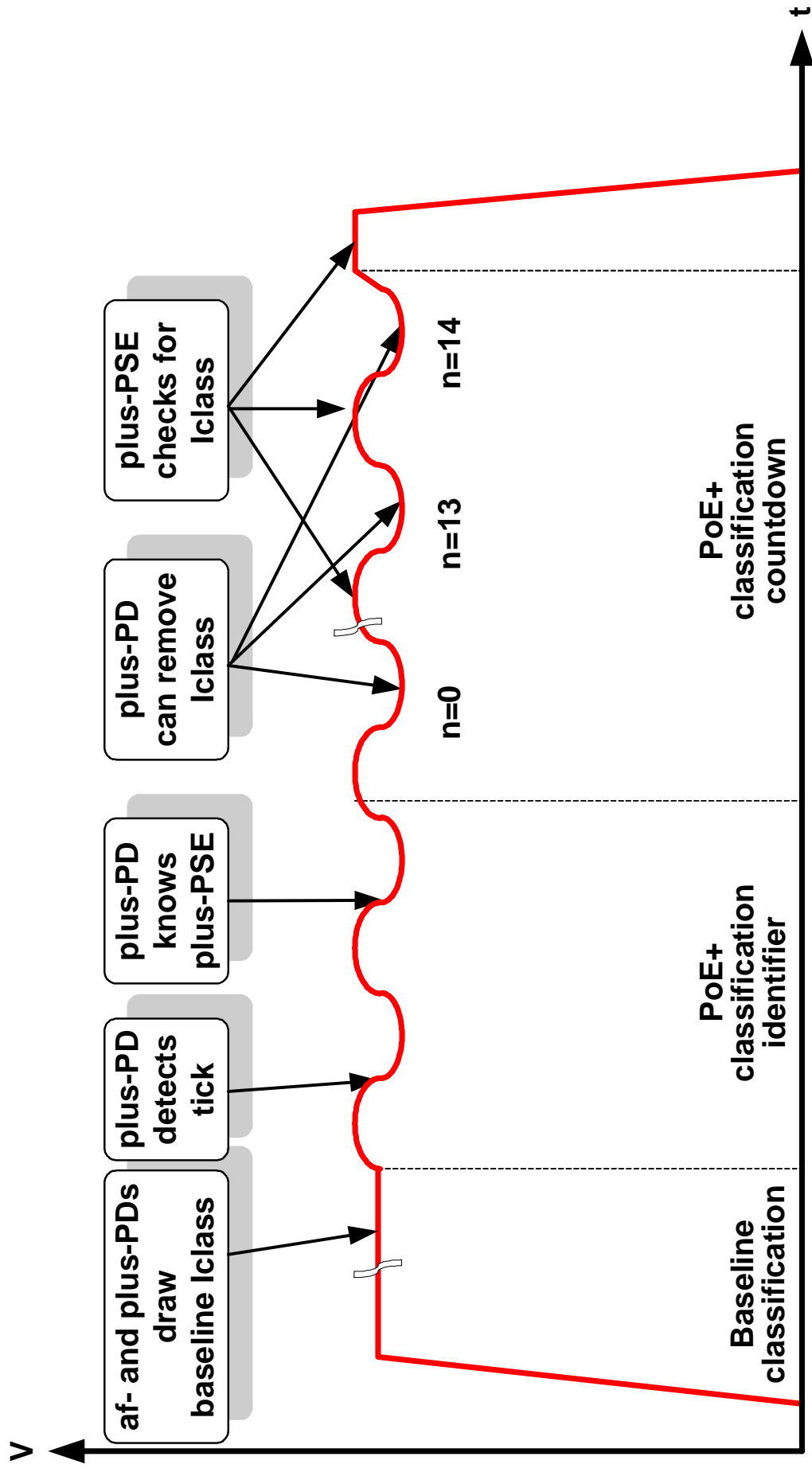
Class	Pmaxlo (W)	Pmaxhi (W)	Step (W)
0	12.95	55.95	2*
1	3.84	6.49	0.177
2	6.49	12.95	0.43
3	12.95	27.95	1
4	12.95	N/A	N/A

- $P_{max} = P_{maxhi} - n * Step$
 - n = number of ticks Iclass is held (0 through 14)
 - If PD does not terminate Iclass, effectively $n=15$
- * final step is 15W for $n=15$

PoE+ Classification Details



PoE+ Classification Details

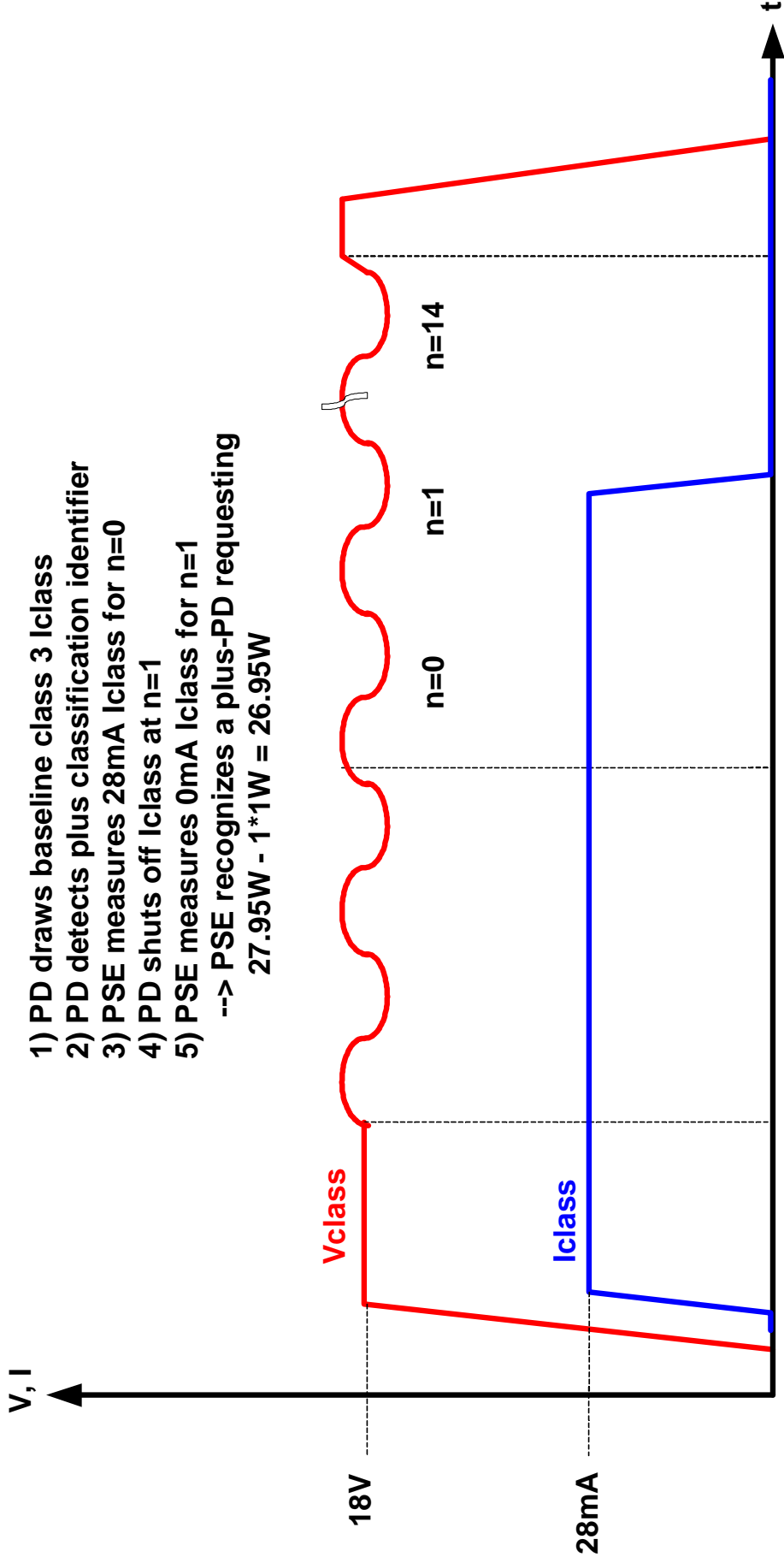


PoE+ Classification Details

- Plus-PD detects falling edge of signal
- Plus-PD either maintains Iclass or removes it during bottom half of duty cycle
- Plus-PSE rechecks Iclass during the following top half of the duty cycle

PoE+ Classification – An Example

- 1) PD draws baseline class 3 Iclass
 - 2) PD detects plus classification identifier
 - 3) PSE measures 28mA Iclass for n=0
 - 4) PD shuts off Iclass at n=1
 - 5) PSE measures 0mA Iclass for n=1
- > PSE recognizes a plus-PD requesting
 $27.95W - 1*1W = 26.95W$



Considerations

- Need to specify a maximum 'Iclassoff' current so plus-PSE knows that a plus-PD has removed current
- Plus-PD could perform tick timing to improve robustness and noise immunity (e.g. if a quick tick or a slow tick is detected, ignore it or shut off Iclass)
 - Relatively tight tick timing accuracy (5%) on plus-PSE allows loose tick capture accuracy on plus-PD
- Class 4 is still left unused
- This class scheme is 2-pair/4-pair agnostic
- Plus-PSE could be required to complete power-up immediately after classification, in order to allow plus-PD not to lose memory

Considerations

- 55.95W max. is arbitrary; can be any number
 - There is an inherent tradeoff between max power, step size, and clock frequency
- Tick frequency could be increased if we want smaller power steps or higher maximum power
- PSE provides all timing
 - Classification levels are exact
 - No cumulative timing error due to inaccurate PD
 - No uncertainty due to asynchronous PD
 - Fixed Iclass measurement period, making data acquisition load deterministic and light
- Safe system response to false edges by down-counting

Does This Meet Objectives 7, 13, & 14?

- Assume 802.3af PSE
 - af-PD will operate normally
 - Plus-PD will not detect 2-tick 'plus Class ID'
 - Will draw Iclass for full tpdcc
 - Default state is to assume af-PSE, so no memory to lose if af-PSE powers down between classification and power-up
 - If power setting falls on lowest end of each baseline class (i.e. n=15 setting), then plus-PD can **always** operate with af-PSE
 - If class setting is some $n < 15$, plus-PD indicates to user that plus-PSE is required

Does This Meet Objectives 7, 13, & 14?

- Assume plus-PSE:
 - af-PD will see valid Vclass, and draw its programmed Iclass for full tpdcc
 - Plus-PSE will think either an af-PD is attached, or a plus-PD is attached that wants minimum power for its class; the distinction does not matter, as their power needs are identical
 - Plus-PD will detect plus Class Identifier
 - Plus-PD counts down ticks, shutting off Iclass when proper count is reached
 - Plus-PSE will know (1) a plus-PD is connected; and (2) what its precise power requirement is

Cost / Complexity

- Plus-PSE:
 - PSEs already monitor voltage and current within the tolerances needed for this classification scheme
 - Most PSEs already inject onto Vport AC signals similar in amplitude and frequency
 - *Additional logic/finite state machine (FSM) complexity is probably negligible*
- Plus-PD:
 - Low-tolerance measurements (tick capture and amplitude) do not require exotic circuit designs
 - Simple FSM, small counters and simple comparators are more or less all that are necessary
 - *Small die area increase, a few inexpensive external passives, and one or two additional pins*



Special Thanks

- Steve Robbins, IXIA
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Thank you

802.3af Classification

- Just for reference (ad nauseum):
 - Vclass 18V \pm 2.5V (14%)
 - Class timing (tpdc) 10 to 75ms
 - Class currents and power levels (@PD):

Class	Iclassmin	Iclassmax	Pmaxlo	Pmaxhi
0	0	4	0.44	12.95
1	9	12	0.44	3.84
2	17	20	3.84	6.49
3	26	30	6.49	12.95
4	36	44	reserved	reserved

802.3af Classification

- The PSE, after detecting a valid signature resistance, applies a voltage V_{class} for time $tpdc$
- The PD must stabilize its classification current within 5ms and maintain it for a duration of $tpdc$
- The PSE measures the current drawn by the PD and classifies it accordingly
- The PSE may choose to remove V_{class} before doing a full powerup, or it may continue ramping V_{port}