An Extended Classification Protocol for PoE Plus (Revised)

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Acknowledgments

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Intro

Purpose of this presentation

To propose an extended classification protocol for PoE Plus that provides high resolution, is relatively simple, and is fully backward-compatible with 802.3af.

Terminology

- Equipment conforming to 802.3af are referred to herein as “af”. Example: “af-PD”.
- Equipment conforming to PoE Plus are referred to as “Plus”. Example: “Plus-PSE”.

Objectives

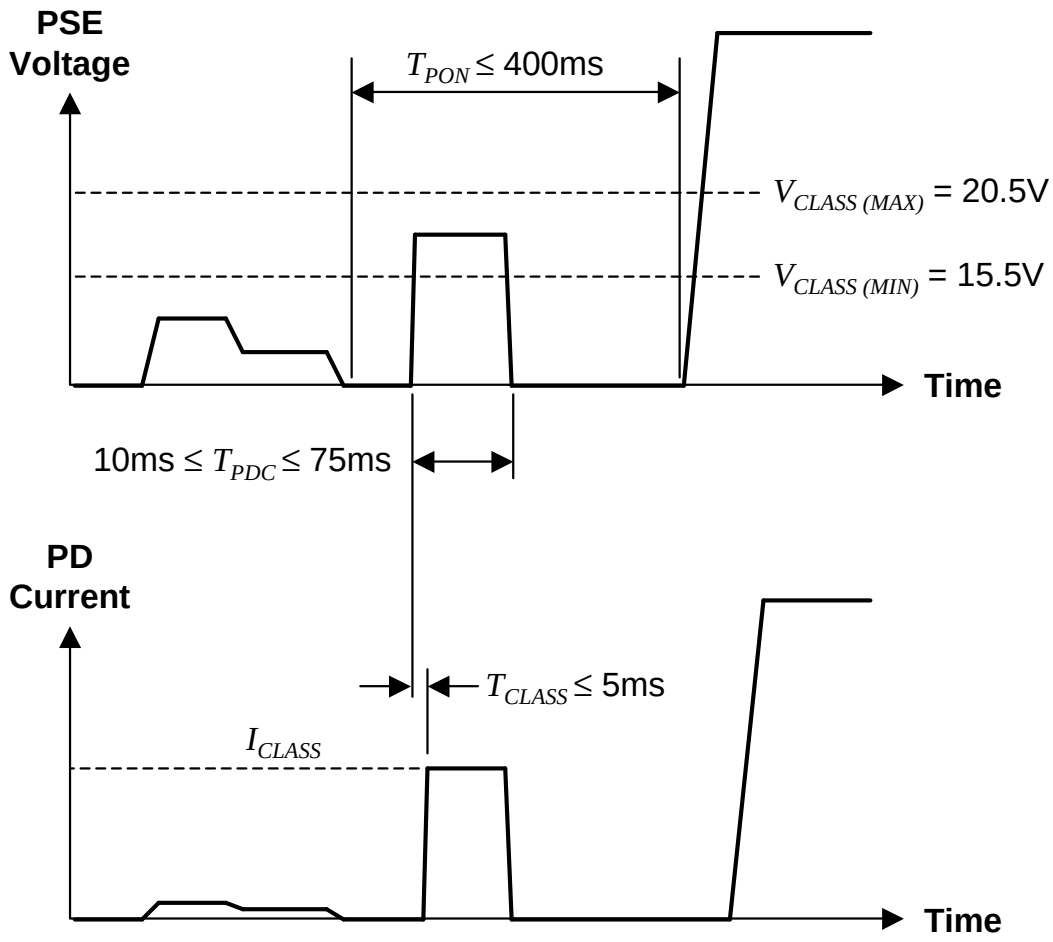
- Higher class resolution – many more power levels
- Mutual identification
  - Plus-PD can identify a PSE as either Plus or af
  - Plus-PSE can identify a PD as either Plus or af
- Backward-compatible with 802.3af
  - Detection signature resistance is not changed
  - af-PSE still able to classify Plus-PD
- Simplicity
  - Does not require serial communication between PSE and PD
  - Does not significantly increase complexity of PD or PSE.

Feedback on Original Proposal

The original proposal, presented at the May meeting in Austin TX, was well received, but there were several concerns:

- Extending the V_{CLASS} period was a concern, because af-PDs are not required to maintain I_{CLASS} beyond 75ms. The scheme depends on af-PD behavior that was undefined in 802.3af.
- Proposed 0.5% timing accuracy was too tight – would increase cost of PD. A low-cost oscillator (using RC timing) was suggested. Frequency accuracy approx 10%.
- Power dissipation during classification, particularly if Class 4 signature (35 to 45mA) were used.

802.3af Classification Protocol

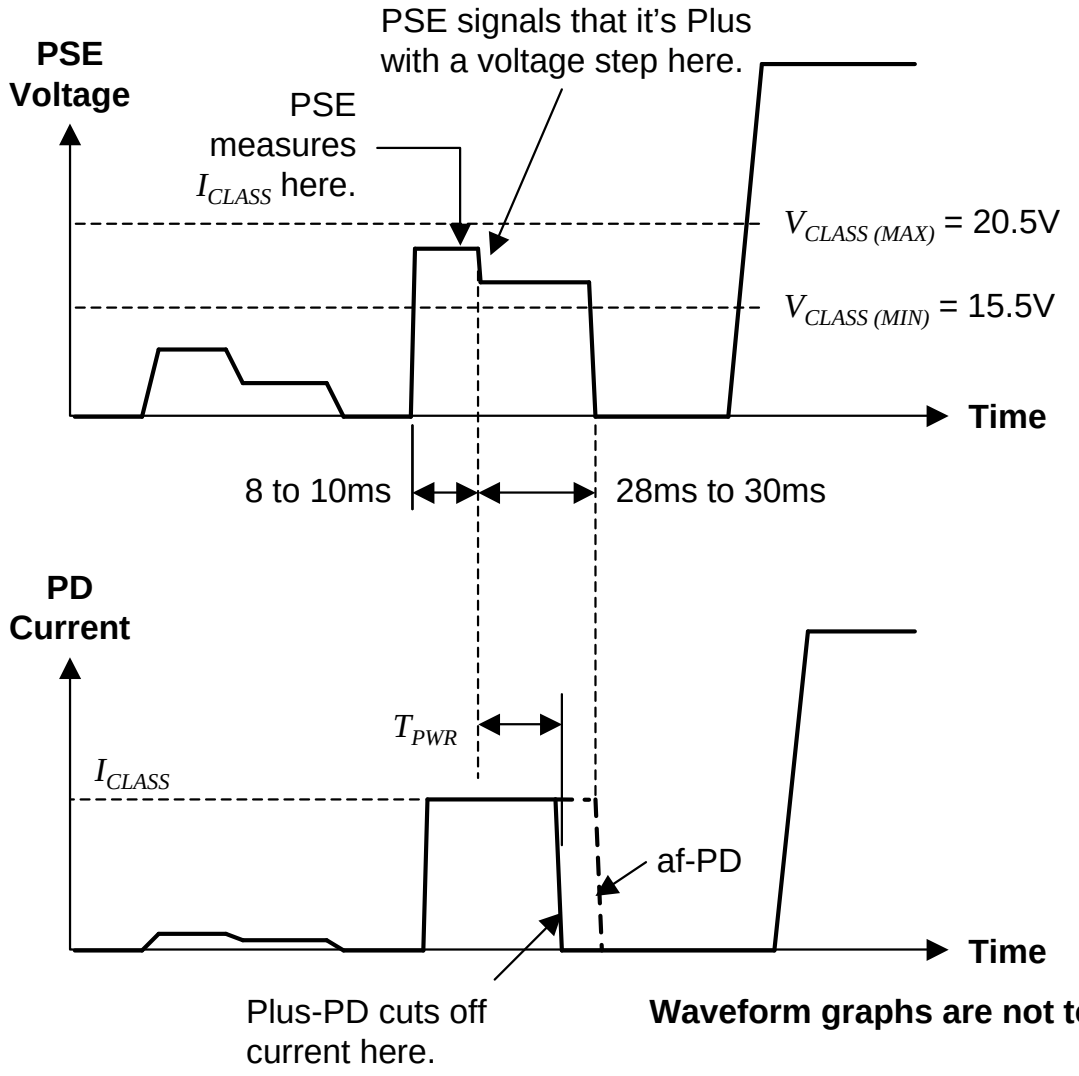


Waveform graphs are not to scale.

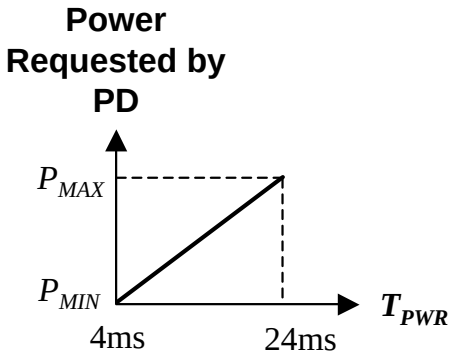
Protocol

1. PSE sources voltage between 15.5V and 20.5V.
2. PD recognizes voltage in this range as a class query. Responds within T_{CLASS} by sinking current I_{CLASS}.
3. PSE measures I_{CLASS}. Determines PD class from Table 33-4.

Extended Classification Protocol



- Plus-PSE steps voltage down but stays within af range.
- Af-PD sinks I_{CLASS} for entire time voltage is in V_{CLASS} range.
- Plus-PD sees step, and starts timing. Cuts off current earlier than the af-PD.
- Plus-PSE measures time from voltage step to I_{CLASS} cut-off.



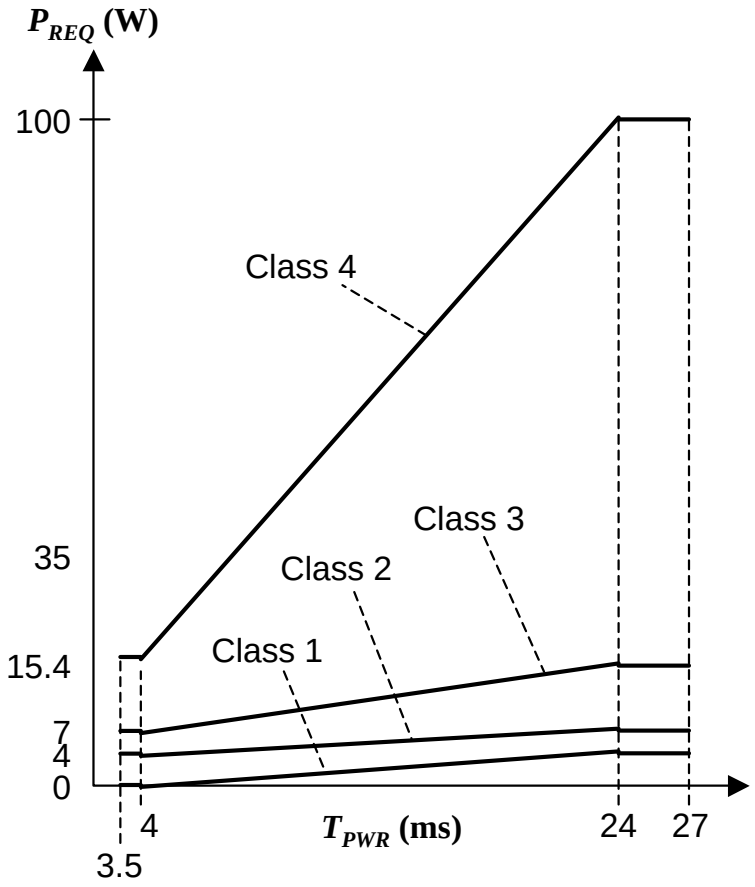
Waveform graphs are not to scale.

Calculating Requested Power

- Both I_{CLASS} and T_{PWR} are measured by Plus-PSE.
- Class is determined from Table 33-4 in 802.3af.
- Requested power (P_{REQ}) is determined from the equations and table below.

$$P_{REQ} = \begin{cases} 0 \text{ (Power Denied)} & T_{PWR} \le 3.5ms \\ P_{MIN} & 3.5ms < T_{PWR} \le 4ms \\ P_{MIN} + (P_{MAX} - P_{MIN})(T_{PWR} - 4ms)/20ms & 4ms < T_{PWR} \le 24ms \\ P_{MAX} & 24ms < T_{PWR} \le 27ms \\ P_{MIN} \text{ (PD is Af)} & 27ms < T_{PWR} \end{cases}$$

Class	P_{MIN}	P_{MAX}
1	1W	4.0W
2	4.5W	7.0W
3	7.5W	15.4W
4	17W	100W



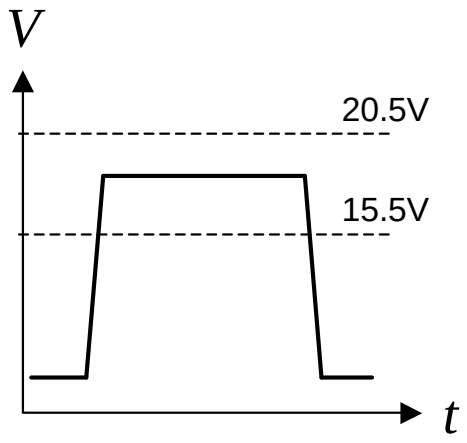
Obvious Questions

Question	Answer
Why is there no Class 0 on the previous slide?	Class 0 is indicated by the *absence* of a signature. No signature current to measure. (The 0 to 5mA range in Table 33-4 simply defines how you know when a signature is absent.)
Why is P_{MAX} so high in Class 4?	So that we never have to do this again. (Assuming there is no way to ever get more than 100W on a CAT-5 cable.)
How might the step affect an af-PD?	The PD classification circuit sees the step as a voltage transient. Settling time is defined for start-up (T_{CLASS}). The two are related by classical control theory. If an Af-PD is perturbed by the step, it's signature current should settle within a few milliseconds.
Why a 20ms-wide timing range?	Parasitic capacitance adds time delay. (See page 15.) A fairly wide range limits the significance of this error.

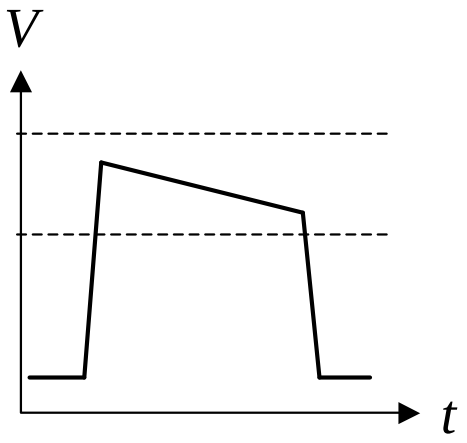
Step Detection Problem

PROBLEM: 802.3af doesn't say anything about the quality of V_{CLASS}, only that it must stay within a specific range.

This is what you would expect from an af-PSE:



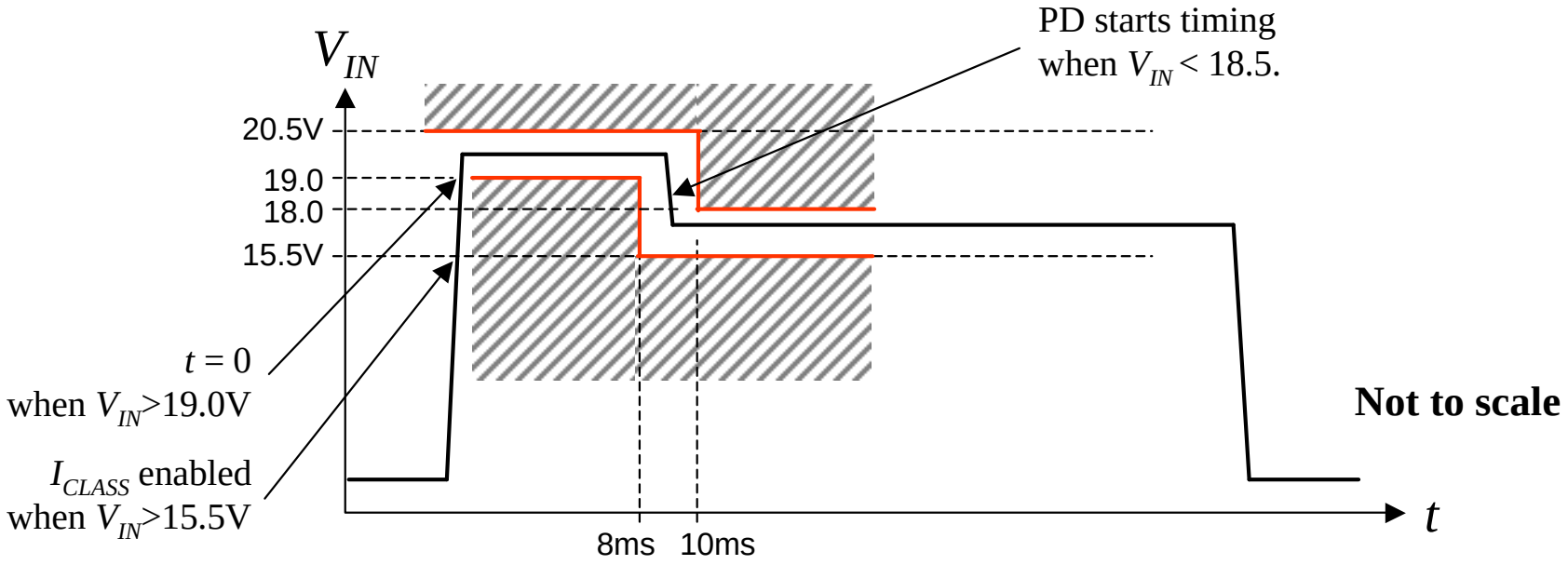
But this is legal too:



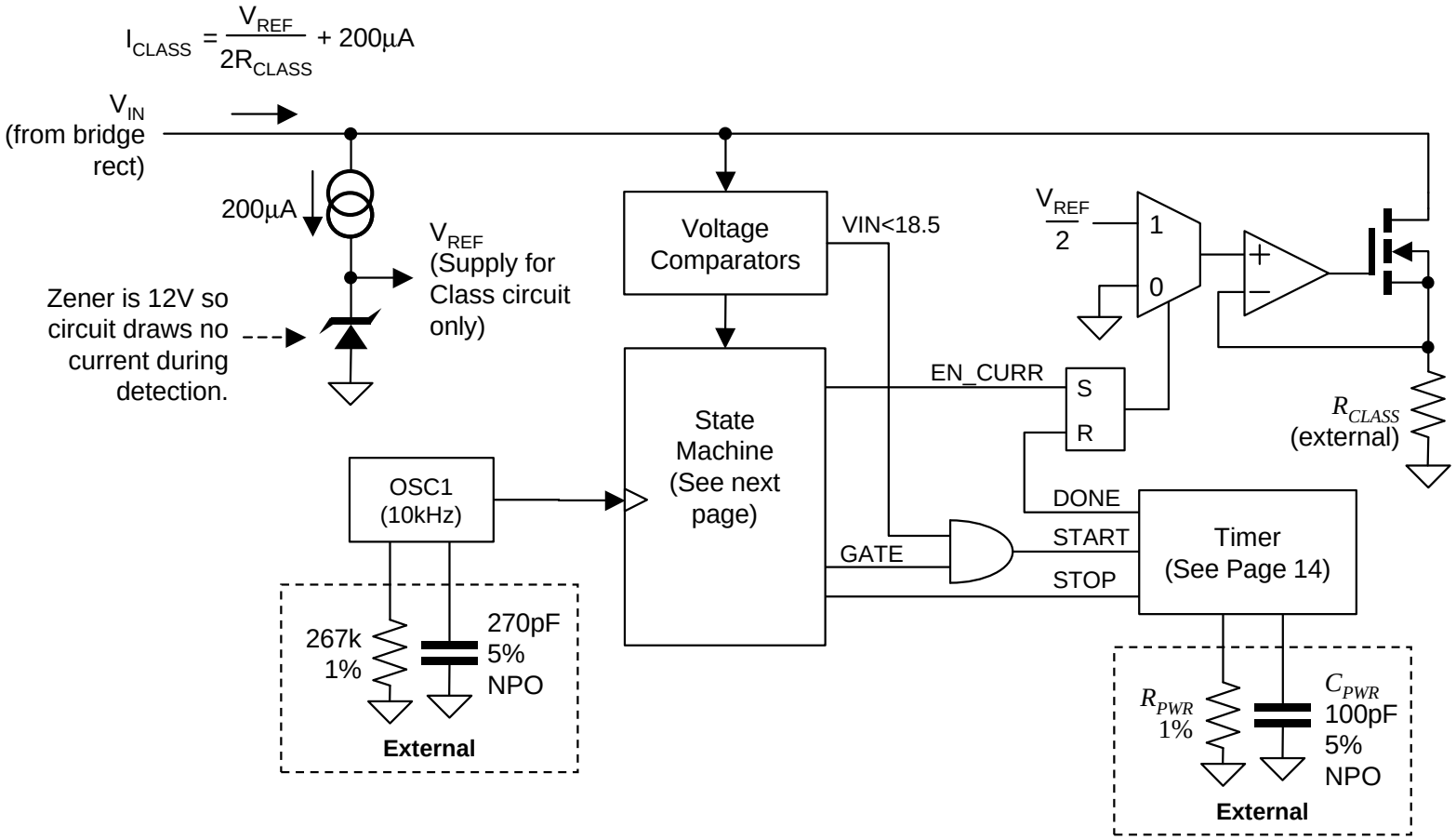
Therefore, a simple hysteretic-type detector (with two voltage thresholds) may not be adequate.

Step Detection Problem

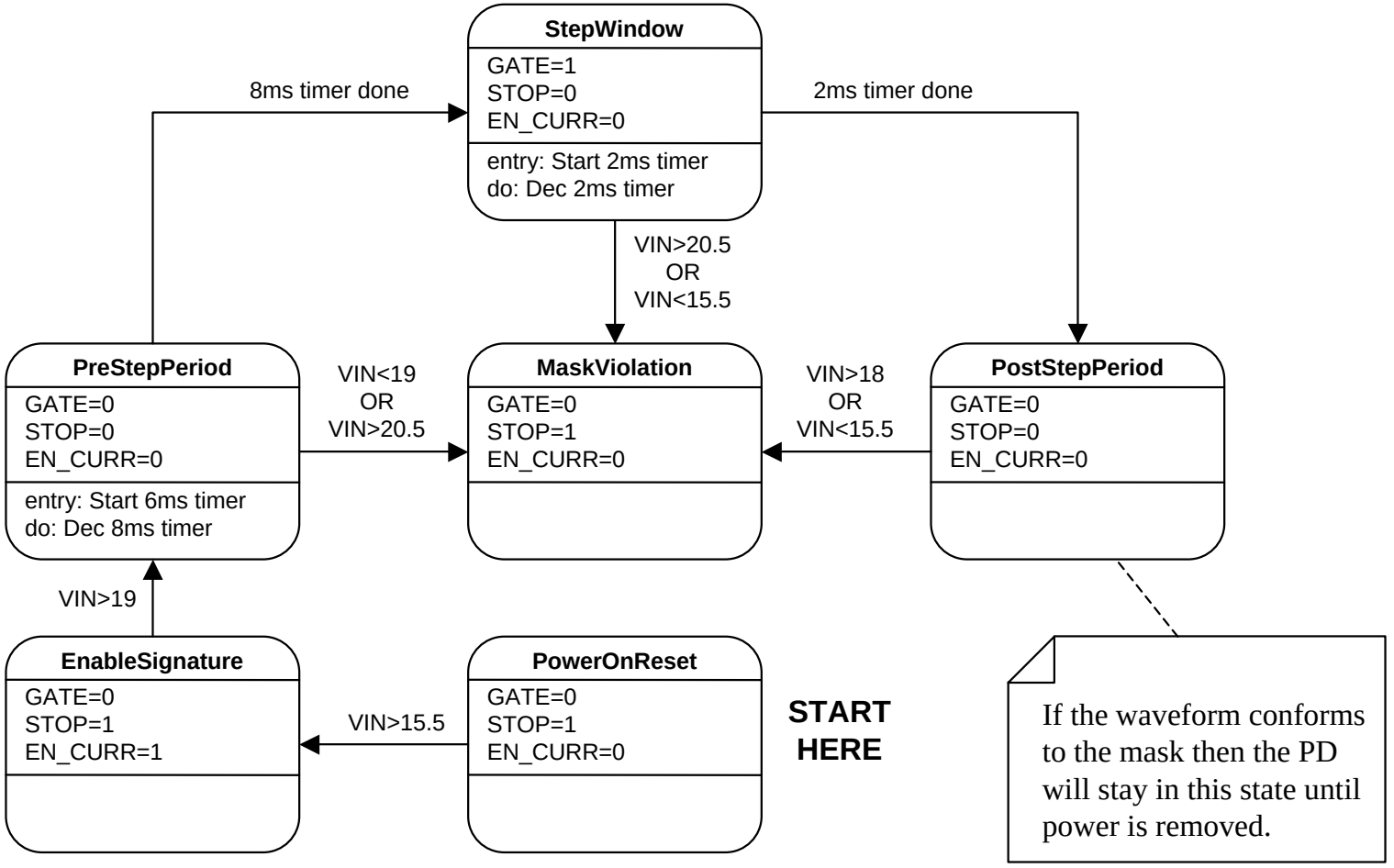
SOLUTION: The PD could use some type of mask test to identify a valid step.



A Possible Plus-PD Design



Plus-PD State Diagram



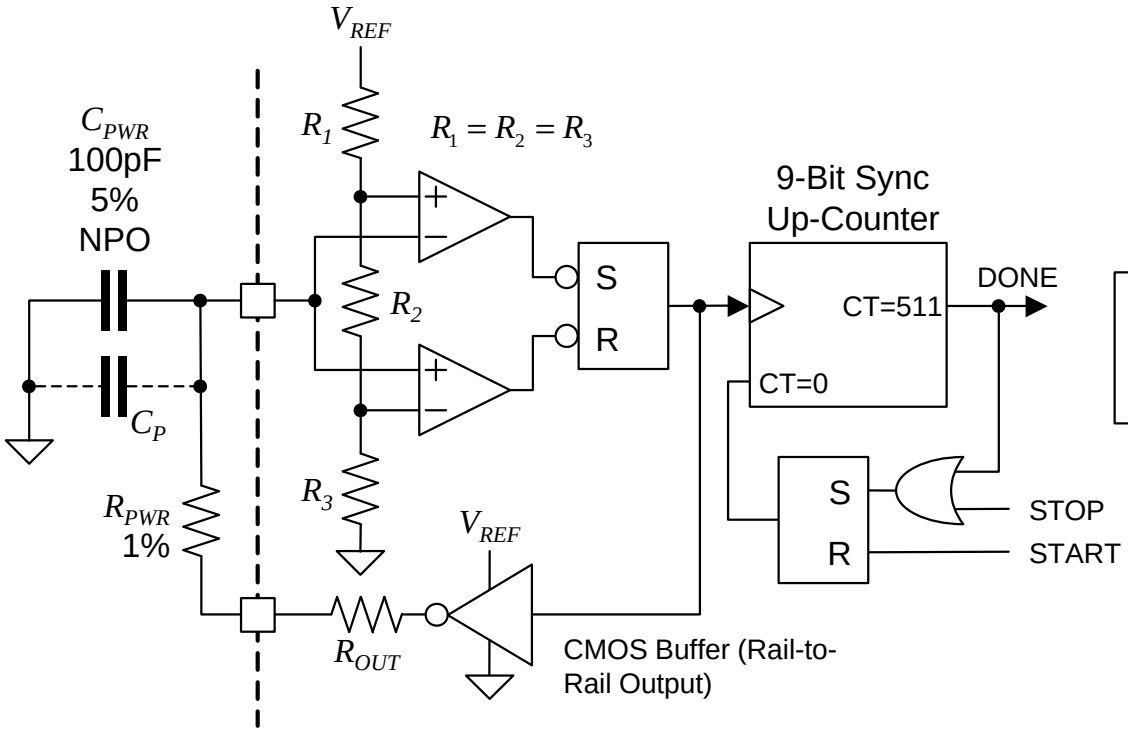
PD Timer Error

A possible PD timer circuit

T_{PWR} is set by varying the oscillator freq rather than the initial state of the counter. This has two advantages:

1. Only two pins are needed.

2. Since the PSE is asynchronous with the PD, the clock period represents quantization error. In this approach the error is a fixed percentage of the T_{PWR}.



Worst-Case Analysis

Assumptions:

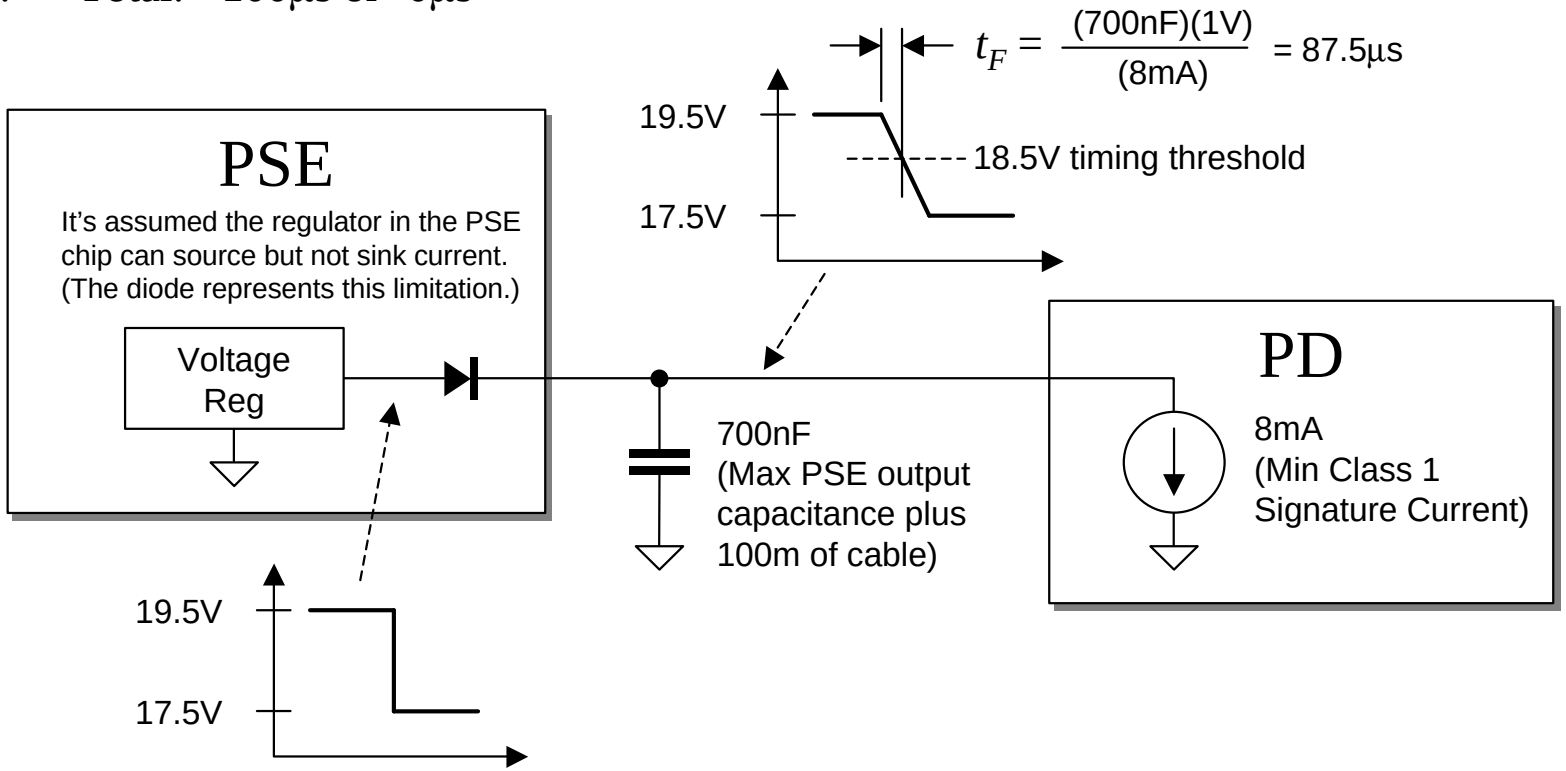
- Resistor ratio matching error ≤ 0.5%
- Parasitic cap (C_P) variation ≤ 2pF
- $R_{OUT} \leq 100\Omega$
- V_{REF} =10V
- Comparator offset mismatch ≤ 10mV
- Total differential delay (comparators, flip-flop, and buffer) ≤ 20ns
- Noise is insignificant

Result:

$$T_{PWR} = (716)R_{PWR}C_{PWR} \pm 7\%$$

Other Timing Error Sources

1. Up to 87.5µs due to capacitance (See diagram below.)
2. PD clock is asynchronous with PSE clock. Assume PSE clock is 80kHz. This means 12.5µs max uncertainty.
3. Total: +100µs or -0µs



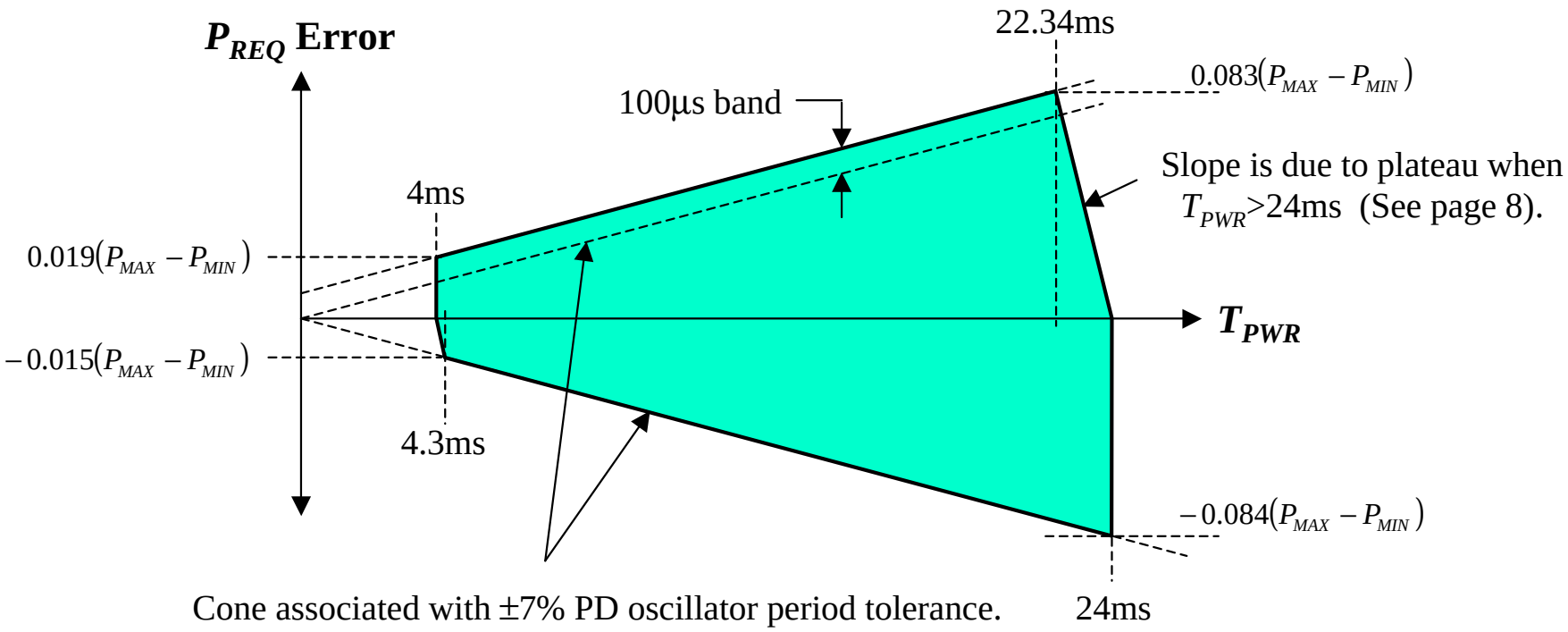
Error Zone for A Single Class

Combined timing error equation: $T_{PSE} = T_{PWR}(1 \pm 0.07)^{+100ms}_{-0}$ ← Combined error due to capacitance and PSE clock period.

Time measured by PSE

Ideal time period (if PD were error-free)

PD Timer tolerance



Cone associated with ±7% PD oscillator period tolerance.
(Assumes PSE oscillator period tolerance is insignificant.)

Sub Classes

Based on worst-case analysis and standard resistor values, we get 11 subclasses.

Sub Class	R_{PWR} (Kohms)	T_{PWR} (ms)			Gaps (ms)	Allocated Power (W)			
		Center	Min	Max		Class 1	Class 2	Class 3	Class 4
0	54.9	3.93	3.66	4.31		1.0	4.5	7.5	17.0
1	68.1	4.88	4.53	5.32	0.23	1.1	4.7	8.1	20.3
2	82.5	5.91	5.49	6.42	0.18	1.3	4.9	8.7	24.2
3	100	7.16	6.66	7.76	0.24	1.5	5.1	9.3	28.9
4	118	8.45	7.86	9.14	0.10	1.7	5.4	10.0	34.5
5	140	10.02	9.32	10.83	0.18	2.0	5.6	10.7	41.2
6	169	12.10	11.25	13.05	0.43	2.3	5.9	11.5	49.2
7	200	14.32	13.32	15.42	0.27	2.6	6.1	12.4	58.8
8	237	16.97	15.78	18.26	0.36	3.0	6.4	13.3	70.2
9	287	20.55	19.11	22.09	0.85	3.5	6.7	14.3	83.8
10	340	24.34	22.64	26.15	0.55	4.0	7.0	15.4	100.0

R_{PWR} values shown assume C_{PWR}=100pF.

Thermal Considerations

- The proposed scheme is harder on the PSE controller chip than 802.3af was:
  - Max I_{CLASS} is higher (Class 4)
  - Min duration is 30ms (was 10ms in 802.3af)
- Implementing the Class 4 signature has an impact on the PD.
  - Worst-case: a Plus-PD could be connected to af-PSE. PD design must be capable of sinking max I_{CLASS} (44mA for Class 4) at max V_{CLASS} (20.5V) for max T_{CLASS} (75ms).
  - Not as bad if connected to a Plus-PSE since V_{CLASS} steps down after 10ms.

Mutual Identification

- How a Plus-PSE determines the PD type:
  - If the PD maintains I_{CLASS} as long as the PSE maintains V_{CLASS} then it's an af-PD.
  - If the PD cuts off I_{CLASS} before the PSE removes V_{CLASS} then it's a Plus-PD.
- How a Plus-PD determines the PSE type:
  - If V_{CLASS} stays constant it's an af-PSE.
  - If V_{CLASS} steps down after 8 to 10ms it's a Plus-PSE.

Backward-Compatibility

- How a Plus-PSE looks to an af-PD:
  - The voltage steps down after about 9ms, but still remains within the range specified in 802.3af.
  - Everything else is the same.
- How a Plus-PD looks to an af-PSE:
  - There is no difference. Voltage and current waveforms look the same.

Cost and Complexity

- Circuitry required in PD:
  - External components: 2 Resistors and 2 Caps
  - PD Controller pin count: +4
  - PD Controller internal circuits:
    - Approx 24 flip-flops, 7 voltage comparators, a few gates.
    - Approx 15 to 20 resistors for various voltage dividers.
- Circuitry required in PSE controller chip:
  - PSE chip already must have a clock input, so no extra pins required. The clock can be shared among all ports, so an oscillator with good precision should not be a significant cost per port.
  - Counter to measure T_{PWR}. Probably 12 bits. But not all bits are ready by software (see page 17).

Issues

- The proposed scheme depends on implementation of the Class 4 signature. An Af-PSE probably won't turn-on a Class 4 PD. So no power for LED.
- Requires 4 (perhaps only 3) extra pins on PD controller chip.
- Worst-case analysis does not yet include voltage margins. Need to add.
- Possible thermal concerns about using Class 4.

Conclusions

- The revised approach addresses the concerns raised at the May meeting.
- Classification up to 100W is achievable with reasonable granularity using low-cost components.
- Practical implementations seem to require at least 3 (probably 4) pins on the PD controller chip:
  - At least 1 (probably 2) pins for the state-machine oscillator
  - At least 2 pins to set the timer.
- Added circuit complexity in both PD and PSE is low.